IC FABRICATION

IC classification - fundamental of monolithic IC technology - epitaxial growth - masking and etching - diffusion of impurities - Realisation of monolithic ICs and packaging - Fabrication of diodes - capacitance, resistance, FETs and PV cell.

Part – A – 2Mark Questions

1. Define an Integrated circuit.

An integrated circuit(IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

2. Give the difference between monolithic and hybrid ICs.

Monolithic IC's	Hybrid IC's
Monolithic IC's are those in which transistors, diodes, resistors are fabricated and interconnected on the same chip.	Hybrid IC's are those in which elements are of discrete form and others are connected on the chip with discrete elements externally to those formed on the chip.

3. Classify IC. (Dec – 14, 15) Or Classify ICs based on the manufacturing techniques. Nov/Dec 2019.
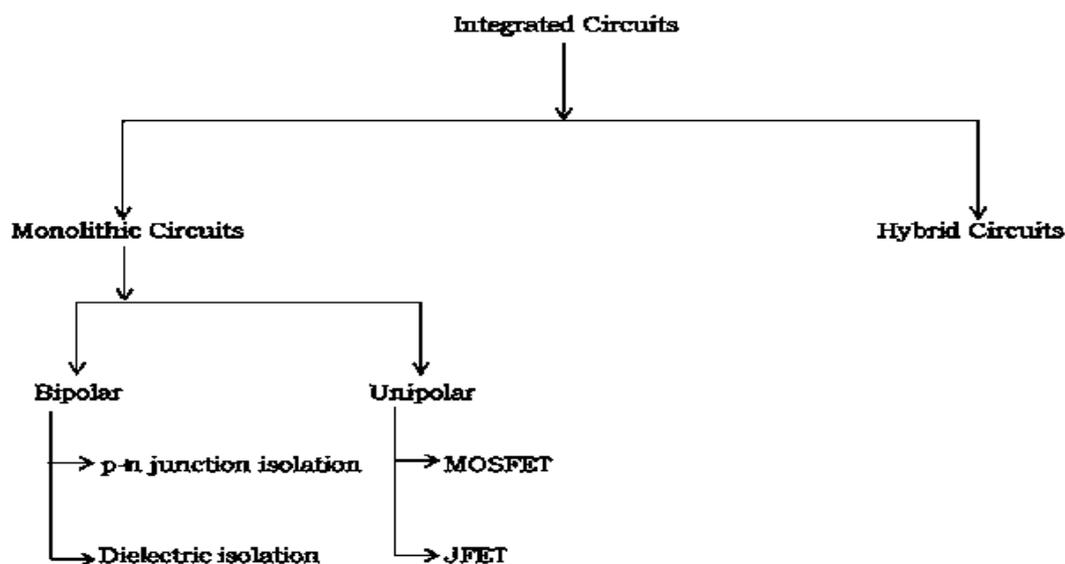
4. List the steps used for preparation of silicon wafer. Nov/Dec 2019.

→ The silicon wafer process can be subdivided into number of sub processes as follows:

    i. Slicing crystal Ingots
    ii. Ingot trimming and grinding
    iii. Ingot slicing
    iv. Wafer etching
    v. Wafer polishing
    vi. Wafer cleaning

5. What is lithography?[May-17, 18]

→ The process of photolithography makes it possible to produce microscopically small circuit and device pattern on Si wafer.

$\rightarrow$ Two processes are involved in photolithography namely,

- ❖ Making a photographic mask
- ❖ Photo etching

$\rightarrow$ The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO$_2$ layer.

6. **What are the advantages of integrated circuits over discrete circuits?(May – 06,15) (Dec – 14, 16) or Name any two merits of ICs. Nov/Dec 2019.**

   Advantages of integrated circuits:

   $\rightarrow$ Miniaturization and hence increased equipment density.

   $\rightarrow$ Cost reduction due to batch processing.

   $\rightarrow$ Increased system reliability due to the elimination of soldered joints.

   $\rightarrow$ Improved functional performance.

   $\rightarrow$ Matched devices.

   $\rightarrow$ Increased operating speeds. Reduction in power consumption

7. **What are the differences between diffusion and ion implantation?**

Diffusion	Ion Implantation
$\rightarrow$ The process of introducing impurities into selected regions of a silicon wafer is called diffusion. $\rightarrow$ The rate at which various impurities diffuse into the silicon will be of the order of 1µm/hr at the temperature range of 900^0C to 1100^0C. Therefore, the impurity atoms have the tendency to move from regions of higher concentrations to lower concentrations. $\rightarrow$ In diffusion process, temperature has to be controlled over a large area inside the oven.	$\rightarrow$ This is a process of introducing dopants into selected areas of the surface of the wafer by bombarding the surface with high-energy ions of the particular dopant. $\rightarrow$ It is performed at low temperature. Therefore, previously diffused regions have a lesser tendency for lateral spreading. $\rightarrow$ In ion implantation process, accelerating potential & beam content are dielectrically controlled from outside.

8. **What is the purpose of oxidation process in IC Fabrication?**

   $\rightarrow$ The process of oxidation consists of growing a thin film of silicon dioxide on the surface of the silicon wafer.

   $\rightarrow$ Silicon dioxide plays an important role in shielding of the surface so that dopant atoms, by diffusion or ion implantation, may be driven into other selected regions.

   $\rightarrow$ SiO$_2$ is an extremely hard protective coating & is unaffected by almost all reagents except by hydrochloric acid. Thus it stands against any contamination.

9. **What is meant by ion implantation? Why is it preferred over diffusion process? (May – 06, 14, 15) (Dec – 12)**

   $\rightarrow$ This is a process of introducing dopants into selected areas of the surface of the wafer by bombarding the surface with high-energy ions of the particular dopant.

   $\rightarrow$ It is performed at low temperature. Therefore, previously diffused regions have a lesser tendency for lateral spreading.

   $\rightarrow$ The ion implantation process is preferred over diffusion because of the following reasons:

        i. The degree of uniformity is maintained same from wafer to wafer.

        ii. The layer can be formed anywhere within substrate.

        iii. The lateral spread is very small.

        iv. The impurity concentration is highly uniform over the wafer.

10. Write the basic chemical reaction in the epitaxial growth process of pure silicon.

$\rightarrow$ The basic chemical reaction in the epitaxial growth process of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$1200^{\circ}C$$
$$SiCl_4 + 2H_2 \xrightarrow{\hspace{1.5cm}} Si + 4\,HCl$$
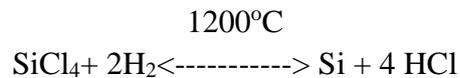
11. List the basic process used in IC fabrication.

$\rightarrow$ The fabrication of a monolithic transistor includes the following steps.

1. Epitaxial growth	6. Emitter diffusion
2. Oxidation	7. Contact mask
3. Photolithography	8. Aluminium metallization
4. Isolation diffusion	9. Passivation
5. Base diffusion	

12. What is parasitic capacitance? (Dec – 04)

$\rightarrow$ In the p-n junction isolation technique, the components on the chip are isolated by forming isolation p-n junction islands.

$\rightarrow$ There are two back to back p-n junction diodes which are under reverse biased condition.

$\rightarrow$ So such reverse bias presents an undesirable and unavoidable capacitance across it.

$\rightarrow$ This is called parasitic capacitance.

$\rightarrow$ This is undesirable as it limits high frequency performance of the circuit.

13. What are the popular IC packages available? (Dec – 03, 06, 13, 15)

    1. Metal can package

    2. Dual-in-line package

    3. Ceramic flat package

14. What is meant by dielectric isolation in I.C Fabrication? Mention its application and Limitations. (Dec – 03)

$\rightarrow$ In dielectric isolation, a layer of solid dielectric such as SiO_2 or ruby completely surrounds each components thereby producing isolation, both electrical & physical.

Limitations:

$\rightarrow$ This method is very expensive due to additional processing steps needed.

Applications:

$\rightarrow$ This is mostly used for fabricating IC's required for special application in military and aerospace.

$\rightarrow$ It is also possible to fabricate both p-n-p &n-p-n transistors within the same silicon substrate.

15. How surface layer of SiO_2 is formed? (Dec – 04)

$\rightarrow$ The surface layer of SiO_2 is formed by oxidation process. In general, thermal oxidation technique is preferred practically to grow thin oxide layers.

$\rightarrow$ Other techniques used are vapour phase oxidation and plasma anodization.

16. What is meant by substantial diffusion? (May – 05)

$\rightarrow$ The process of adding impurities to the silicon chip at very high temperature is called substantial diffusion.

17. What is the need for buried layer in fabrication of monolithic integrated transistor? (Dec – 07) (Dec – 14)

$\rightarrow$ The buried layer is used in integrated transistor to decrease the collector series resistance. It provides low resistivity current path.

$\rightarrow$ The buried n+ layer shunts the n-epitaxial collector layer effectively, decreasing the resistance.

18. Differentiate between thin film and thick film technology in IC fabrication. (Dec – 07)

$\rightarrow$ Generally thick-thin film ICs are used to produce only passive elements.

$\rightarrow$ The thick film technology is comparatively easier and inexpensive while the thin film technology is slightly complicated and expensively.

$\rightarrow$ The thin film technology produces components with greater precision as compared to those produced by the thick film technology.

19. List the advantages of thin film resistor. [Apr/May 2019]

Thin film is usually used for precision applications.

$\rightarrow$ High Tolerances

$\rightarrow$ Low Temperature Coefficients

$\rightarrow$ Low Noise

20. Define the term epitaxial growth.

$\rightarrow$ Epitaxial means growing a mono-crystalline film on top of a mono-crystalline surface.

$\rightarrow$ Thus Epitaxial is a crystalline growth process in which the foundation layer i.e. substrate works as a seed crystal.

21. What do you mean by Monolithic process? (Dec – 06)

$\rightarrow$ The process in which all the active as well as passive elements or components along with their interconnections are manufactured on a single silicon crystal is known as monolithic process.

22. What is meant by hybrid ICs?

$\rightarrow$ The hybrid ICs are the integrated circuits used for high power application.

$\rightarrow$ The hybrid ICs may combine two or more monolithic ICs or combine monolithic ICs with thick-thin film IC in one single package.

23. What is meant by planar technology?

$\rightarrow$ The fabrication of different discrete devices such as diodes, transistors and integrated circuits is carried out by the same technology.

$\rightarrow$ The various processes involved in the fabrication of different devices are carried out in a single plane. Hence this is also referred as a planar technology.

24. Name the parameters which govern the thickness of the film in the oxidation process. (Dec – 05)

$\rightarrow$ The main important parameter which governs the thickness of the film in the Oxidation process is Temperature.

$\rightarrow$ This is because, to grow the oxide layer, high temperature is to be maintained.

$\rightarrow$ The other important parameters which govern the thickness of the film in the Oxidation process are time till which the process is to be carried out and the moisture contents.

25. How are capacitors fabricated in ICs? Draw the cross-sectional view of M0S capacitor. (May – 07)

$\rightarrow$ The common parallel plate capacitor structures area shown in the Fig.

$\rightarrow$ In most widely used type shown in Fig. (a), the two poly-silicon plates are separated by silicon dioxide (SiO_2).

$\rightarrow$ Here the lower plate rests on the top of the Substrate.

$\rightarrow$ The capacitor shown in Fig. (b) is MOS capacitor.

$\rightarrow$ It consists of an implanted or diffused heavily doped layer within substrate while a poly-silicon or metal plate on the top of a thin oxide layer.

→ For MOS capacitors, generally gate oxide is used with no extra processing step.

(a) Poly-poly capacitor
(b) Poly-metal capacitor

Capacitor structures
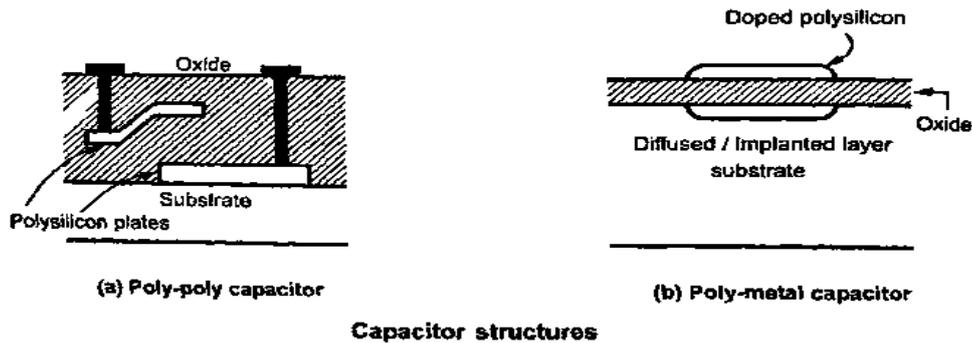
26. What are the limitations of Integrated Circuits? (May – 07) (Nov-16, 17)

→ The disadvantage if ICs are,

    i. The capacitors more than 30 pF cannot be fabricated.
    ii. The resistors more than 100 kΩ cannot be fabricated.
    iii. The coils or inductors cannot be fabricated.
    iv. The ICs can handle limited amount of power.
    v. The ICs function at low voltages.

27. Explain the importance of SiO_2 layer. (May – 06)

→ In the planar process it is essential to protect certain regions of surface of the wafer so that the dopant atoms may be driven into other selective regions during the processes such as diffusion or ion implantation.

→ For such shielding purpose, silicon dioxide (SiO_2) is best suited.

28. In the Czochralski crystal growth process under what gas does crystal pulling carried out? (May – 05)

→ In general, during Czochralski crystal growth process, the gas used is argon.

29. What is the advantage of using dry etching process? (May – 05)

→ The major advantage of using the dry etching process over wet etching process is that it is possible to achieve smaller openings of thickness ≤ 1 μm.

30. What is the step taken to avoid material defect in ion implantation? (May – 05)

→ To avoid the material defect in the ion implantation process, the depth of penetration must be controlled appropriately by the acceleration energy of the incident beam and the doping concentration.

31. Distinguish between dry etching and wet etching. (May-15)

Wet etching process, the chemical reagents are used are liquid form. Dry etching process, it is achieve smaller line openings compared to wet process.

32. What are the advantages of plasma etching? (Nov-13)

It is possible to achieve smaller line openings compared to wet process.

33. Define Encapsulation. [Apr/May 2019]

In electronics manufacturing, integrated circuit packaging is the final stage of semiconductor device fabrication, in which the block of semiconductor material is encapsulated in a supporting case that prevents physical damage and corrosion.

IC FABRICATION

Part – B – 16Mark Questions

FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

Integrated Circuits:

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.
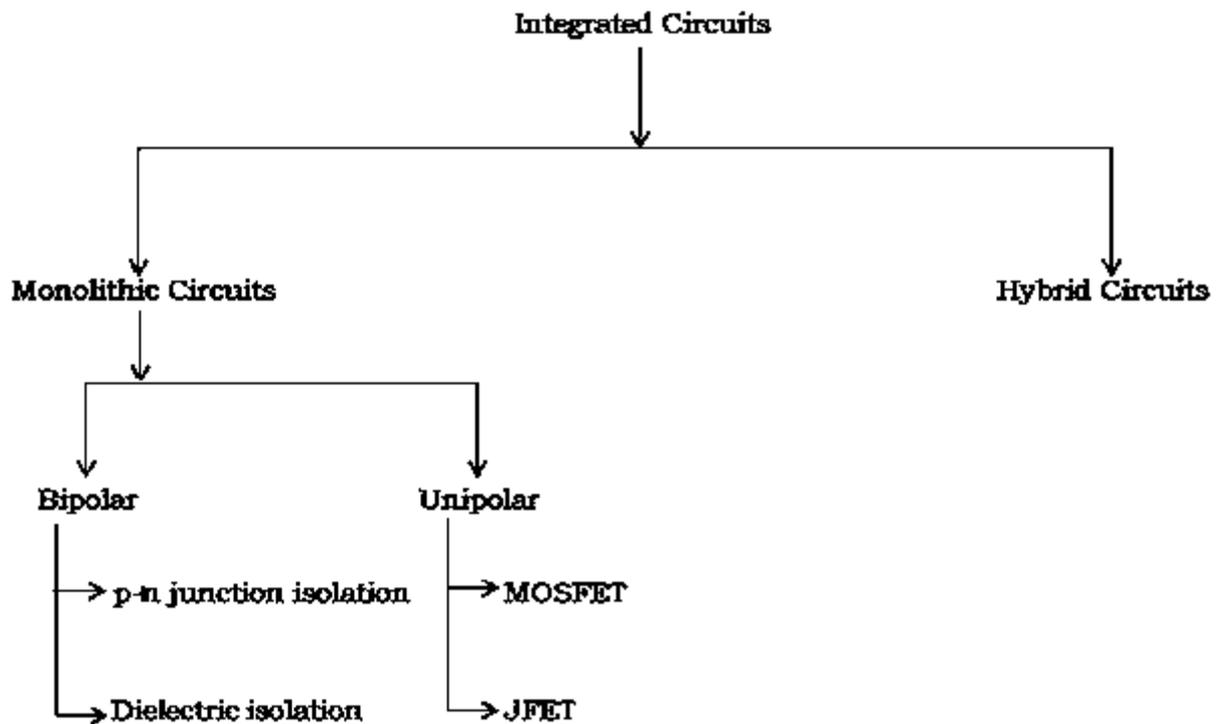
Advantages of integrated circuits:

→ Miniaturization and hence increased equipment density.
→ Cost reduction due to batch processing.
→ Increased system reliability due to the elimination of soldered joints.
→ Improved functional performance.
→ Matched devices.
→ Increased operating speeds.
→ Reduction in power consumption.

1. Write short notes on classification of IC.

1. IC Classification:

→ Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip).

→ Based upon above requirement two different IC technologies namely Monolithic Technology and Hybrid Technology have been developed.

→ In monolithic IC, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon.

→ In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.

→ Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimetres.

→ The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level integration.

→ These digital ICs, typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

→ Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc.

→ Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

→ ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters.

→ Such circuits offer smaller size and lower cost, but must carefully account for signal interference.

1.1 Classification of ICs:

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                        Integrated Circuits
                               │
                               ▼
        ┌──────────────────────────────────────────┐
        ▼                                            ▼
  Monolithic Circuits                          Hybrid Circuits
        │
        ▼
   ┌──────────────────┐
   ▼                  ▼
 Bipolar           Unipolar
   │                  │
   ├→ p-n junction    ├→ MOSFET
   │   isolation      │
   │                  │
   └→ Dielectric      └→ JFET
      isolation
```

1.2 Generations:
SSI, MSI and LSI

→ The first integrated circuits contained only a few transistors. Called **"Small-Scale Integration"** (SSI), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors.

→ The term **Large Scale Integration** was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI. They began to appear in consumer products at the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

→ The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called **"Medium-Scale Integration" (MSI).**

→ They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

VLSI

→ The final step in the development process, starting in the 1980s and continuing through the present, was **"very large-scale integration" (VLSI).**

→ The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

→ In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors.

→ Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005 ULSI, WSI, SOC and 3D-IC.

→ To reflect further growth of the complexity, the term ULSI that stands for "Ultra-Large Scale Integration" was proposed for chips of complexity of more than 1 million transistors.

→ Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip".

→ Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably massively parallel supercomputers.

→ The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

→ **System-on-a-Chip (SoC or SOC)** is an integrated circuit in which all the components needed for a computer or other system is included on a single chip.

→ The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements.

→ However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget, because signals among the components are kept on-die, much less power are required.

→ **Three Dimensional Integrated Circuits (3D - IC)** has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit.

→ Communication between layers uses on-die signalling, so power consumption is much lower than in equivalent separate circuits.

→ Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

2. FUNDAMENTAL OF MONOLITHIC IC TECHNOLOGY
2.1 WAFER PREPARATION

2. Describe the steps of crystal growth and wafer preparation in detail. (May – 05) (4)

→ The most important process in IC fabrication is the formation of a silicon wafer through crystal growth.

→ This process can be subdivided into number of sub processes as follows:

       vii.   Slicing crystal Ingots
     viii.   Ingot trimming and grinding
       ix.   Ingot slicing
        x.   Wafer etching
   xi.   Wafer polishing
      xii.   Wafer cleaning

1. Slicing Crystal Ingots:

→ The important semiconductor material for the fabrication of semiconductor devices and integrated circuits is **silicon**.

→ Other semiconductor materials are **germanium** and **gallium arsenide**.

→ At present 95% of the semiconductor devices and integrated circuits are manufactured using silicon only and for very special applications gallium arsenide is preferred.

→ It is seen that the bipolar junction transistor (BJT) was developed first in 1948, with germanium as a basic semiconductor material.

→ But it was observed that silicon is better option than germanium.

→ The comparison between silicon and germanium is as given in Table.

Sl. No.	Germanium	Silicon
1.	It is unsuitable for certain application due to high junction leakage currents as it has currents relatively narrow energy band gap (0.66 eV).	It is comparatively suitable for all applications as junction leakage currents are negligible as the energy band gap is comparatively broader (1.1 eV).
2.	Germanium devices can be operated till 100°C temperatures.	Silicon devices can be operated till 200°C temperatures.
3.	Germanium oxides are unsuitable for certain device applications.	Silicon dioxides are the most wanted for the planar processes.
4.	The intrinsic resistivity without any dopantis 47 Ωcm, hence not suitable for high voltage rectifying devices.	The intrinsic resistivity Without any dopantis 230,000 Ωcm, hence most suitable for high voltage rectifying devices as well as infrared sensing devices.
5.	Germanium is costlier as compared to Silicon.	Silicon is cheaper as compared to Germanium.

→ The primary method of the crystal growth is Czochralski (CZ) method.

→ In practice all the silicon required for integrated circuits is prepared by using this method only.

→ In general, a phase change from solid, liquid or gas phases to crystalline solid phase is nothing but growing crystal.

→ Czochralski method is used for silicon crystal growth from which ultimately silicon wafers are produced.

→ The apparatus used for the crystal growth is called Czochralski crystal growth apparatus or puller.

→ The puller has four important subsystems namely furnace, crystal pulling mechanism, ambient control and control systems.

→ The simplified version of Czochralski crystal puller is as shown:

→ The furnace consists of a crucible, crucible support, rotation mechanism and heating element housed in a chamber.

→ The crucible is made up of fused silica (SiO_2) as this material is chemically un reactive with molten silicon.

→ An EGS block is heated in a fused silica crucible with the appropriate dopant using a heating element.

→ The material in the crucible is heated to a temperature which is greater than the melting point of silicon, i.e. 1417°C.

→ A resistance heating is preferred for large pullers; while induction heating is used for small melt sizes.

→ Then a small single crystal rod of silicon is immersed into the molten material.
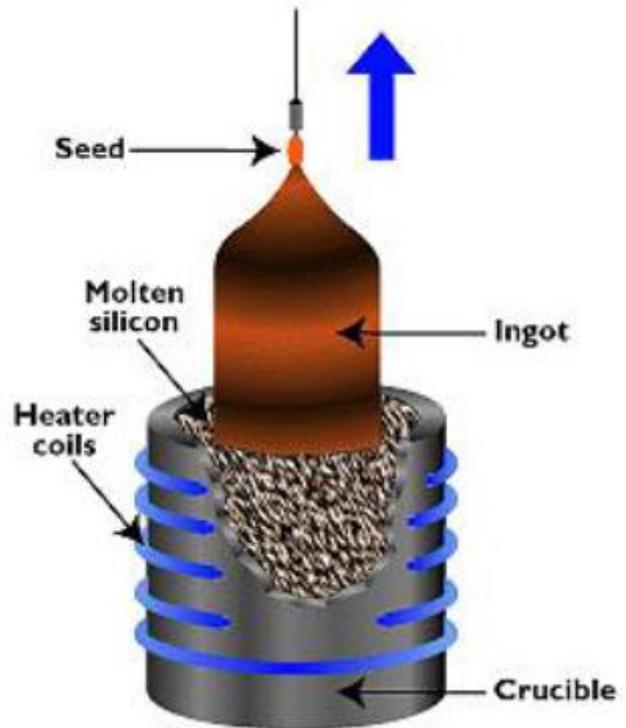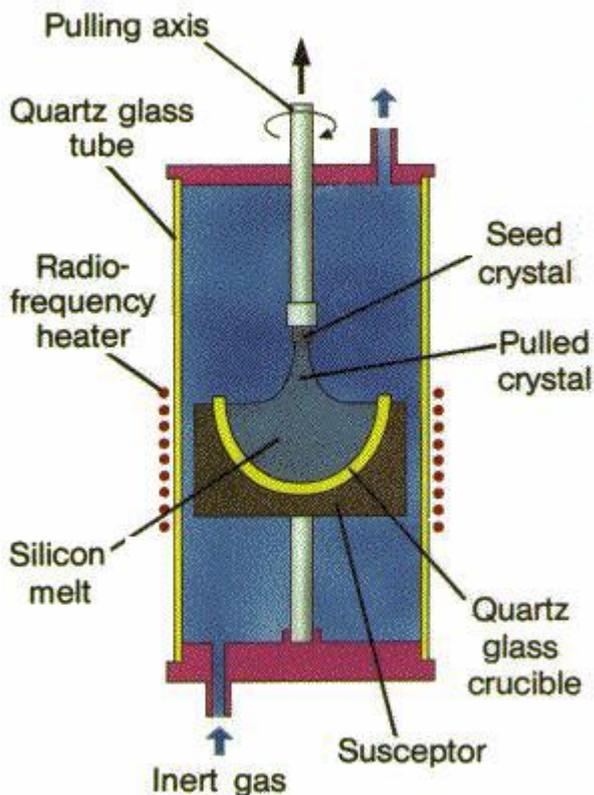
→ This rod is called seed crystal. This seed crystal is located at the crystal pulling assembly.

→ In this assembly, using rotating mechanism seed shaft and seed chuck are rotated.

→ Lowering the seed crystal in molten silicon allows the crystal ingot to form on the seed by solidification.

→ The main function of crystal pulling assembly is to control the pull rate of seed crystal and crystal rotation both, with minimum Vibrations and precision.

→ During the crystal growth, the crystal is rotated slowly, by stirring the molten and averaging out temperature gradients leading to inhomogeneous solidification.

→ To get the ingots of circular cross-section, the crucible and the seed crystal are rotated in opposite direction.

→ When the seed crystal is pulled out of the molten material, due to solidification, silicon ingot gets formed exactly same as seed crystal.

→ In general, the diameter is controlled by the pull rate.

→ The standard diameter of the ingot is about 150 mm and the length is about 2 m.

→ The ingot with such dimensions weighs about 60 kg.

→ The silicon growth is generally conducted in a vacuum or in an inert gas like helium or argon.

→ To control the process parameters such as temperature, crystal diameter, pull rate and rotation speed etc, control system is used which works under either open loop control or closed loop control.

2. Ingot trimming and grinding:

→ First of all, the seed which initiated the crystal growth is separated from the circular ingot.

→ The top and bottom ends are also cut off. As silicon is hard and brittle material, industrial grade diamond is used for shaping and cutting it.

→ This process is called ingot trimming. After completion of the crystal growth, it is generally tested for resistivity and perfection evaluation.

→ So the portions of the ingot failed in the above tests are also cut.

→ Note that these cuttings can be recycled for new crystal growth after cleaning.

→ After trimming of the ingot, the surface grinding of the ingot is carried out.

→ Actually the ingots are slightly oversized. Hence with the help of lathe like diamond tool, the ingot is ground to a precise diameter.

→ After grinding the ingot to a precise diameter, generally two flats are ground along the length of the ingot.

→ The larger flat is called major or primary flat and it is positioned relative to the crystal direction.

→ The X-ray technique is used to locate the primary flat.

→ The primary flat is very important as,

i) It serves for mechanical alignment of the wafer in automatic processing, and

ii) It serves for orienting ICs on the wafer relative to the crystal.

→ The smaller flat is called **secondary** flat which is used to identify the orientation ($< 100 >$ or $< 111 >$) and conductivity (p or n) of the wafer.

3. Ingot slicing:

→ After completing ingot trimming and grinding process, the ingot is ready for next process i.e. ingot slicing.

→ The slices of the ingot are called wafers and typically the thickness of wafer may vary from 0.4 mm to 1 mm.

→ This process is very important as it is necessary to maintain the flat plane and desired surface orientations.

→ The slicing also determines the orientation of the surface. Generally, there are two orientations $<100>$ and $<111>$.

→ The wafers with $<100>$ are cut **'on orientations'** and wafers with $<111>$ are cut **'off orientations'**.

→ The ingot is sliced using a circular cutting blade kept in tension on the outer edge while having the cutting edge on the inner diameter.

→ The thickness of the wafer is determined by the slicing.

→ It is another important wafer parameter because thicker wafers can easily withstand the stresses of subsequent thermal processes.

→ The higher quality of slicing is achieved by using capacitive sensing device near the blade which helps the blade to be positioned correctly to achieve exactly flat plane cut.

4. Wafer etching:

→ If the sliced wafers are to be used for VLSI application, then before etching process two sided mechanical lapping process is carried out.

→ Using this process, wafers with uniform flatness are achieved which are mostly required for photolithography.

→ Due to the machining operations during trimming, grinding and slicing, the surface and edges of the wafers get contaminated and even damaged.

→ The depth of damage depends on the mechanical operations carried previously.

→ It is observed that the damaged and contaminated regions are not more than 10 µm deep.

→ Even by using chemical etching process, all the damaged and contaminated edges can be removed.

→ Practically mixture of hydrofluoric, acetic and nitric acids is used in chemical etching. This is called acidic etching.

→ The other alternative is to use alkaline etching using potassium hydroxide or sodium hydroxide.

→ By the etching process, typically 10 µm to 30 µm of wafer is removed from both the sides.

5. Wafer polishing:

→ After etching, the wafer is polished to eliminate the micro-cracks and debris.

→ The main intension of polishing a wafer is to provide a smooth and perfect flat surface such that the device features can be engraved.

→ The polishing is done with the help of a polishing machine. Note that the polishing process removes further 10 µm to 30 µm of the wafer surface typically.

→ The three steps of lapping, etching and polishing reduce the wafer thickness by 40 to 150 µm.

→ Thus by considering the typical figures, to have the wafer of 200 µm thickness, the thickness of the substrate required is 560 µm.

→ In practice, the processed 6 inch wafers are typically 250 µm to 500 µm thick.

6. Wafer cleaning:

→ The silicon wafers are cleaned using chemicals.

→ Generally organic films, heavy metals are deposited on the surface of the wafers.

→ Hence by using HCl - H_2O_2 aqueous solution, metallic impurities can be removed.

→ First the wafer is cleaned by using HCl - H_2O_2. Then wafer is rinsed in water to deionise.

→ Again the wafer is dipped in hydrofluoric acid. Then again the wafer is rinsed in water.

→ After cleaning process, the wafer is ready for the formation of the dies.

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3. Explain the basic Process used in silicon planar technology with neat diagram. (Nov-17) (16, 13)

Or

Describe the methods of thin thick film technologies [Apr/May 2019]

Or

Explain the basic processes used in the fabrication of monolithic ICs. (Dec – 12) (16)

Or

Discuss with necessary diagram, the basic process for fabrication of ICs using silicon IC planar technology. Nov/Dec 2019. (13)

2.2 CONSTRUCTION OF A MONOLITHIC BIPOLAR TRANSISTOR:

→ The fabrication of a monolithic transistor includes the following steps:

1. Epitaxial growth
2. Oxidation
3. Photolithography
4. Diffusion
    i. Isolation diffusion
    ii. Base diffusion
    iii. Emitter diffusion
5. Ion implantation
6. Isolation Technique
7. Contact mask
8. Aluminium metallization
9. Passivation

$\rightarrow$ The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

2.2.1 EPITAXIAL GROWTH

4. Explain the epitaxy and explain epitaxial growth process. (Dec – 03, 06, 10, 13, 16) (4, 6, 8)
Or
Explain the process of epitaxial growth in IC fabrication process with neat diagram. (May – 07, 15) (8)

1. Epitaxial growth:

$\rightarrow$ Epitaxy means growing a single crystal silicon structure upon an original silicon substrate, so that the resulting layer is an extension of the substrate crystal structure.

$\rightarrow$ The basic chemical reaction in the epitaxial growth process of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$1200^{o}C$$
$$SiCl_4 + 2H_2 \longleftrightarrow Si + 4\ HCl$$

$\rightarrow$ The first step in transistor fabrication is creation of the collector region.

$\rightarrow$ It normally requires a low resistivity path for the collector current.

$\rightarrow$ This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.

$\rightarrow$ The higher collector resistance is reduced by a process called buried layer as shown in figure.

$\rightarrow$ In this arrangement, a heavily doped N region is sandwiched between the N-type epitaxial layer and P – type substrate.

$\rightarrow$ This buried N+ layer provides a low resistance path in the active collector region to the collector contact C.

$\rightarrow$ In effect, the buried layer provides a low resistance shunt path for the flow of current.

Epitaxial layer
(N layer)
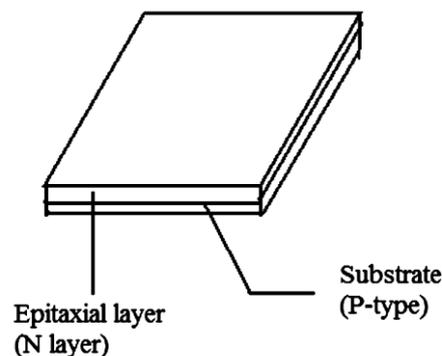
Substrate
(P-type)

$\rightarrow$ For fabricating an NPN transistor, we begin with a P-type silicon substrate having a resistivity of typically 1Ω-cm, corresponding to an acceptor ion concentration of 1.4×10^{15} atoms/cm^3.

$\rightarrow$ An oxide mask with the necessary pattern for buried layer diffusion is prepared.

$\rightarrow$ This is followed by masking and etching the oxide in the buried layer mask.

$\rightarrow$ The N-type buried layer is now diffused into the substrate.

$\rightarrow$ A slow-diffusing material such as arsenic or antimony is used, so that the buried layer will stay-put during subsequent diffusions.

$\rightarrow$ The junction depth is typically a few microns, with sheet resistivity of around 20Ω per square.

→ Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at 1200^0 C and introducing a gas containing phosphorus (donor impurity).

→ The subsequent diffusions are done in this epitaxial layer.

→ All active and passive components are formed on the thin N-layer epitaxial layer grown over the P-type substrate.

5. Explain the importance of SiO₂ layer. (May – 06) (8)

Or

Describe the steps of oxidation in IC fabrication. (May – 05) (4)

2.2.2 Oxidation:

→ The process of oxidation consists of growing a thin film of silicon dioxide on the surface of the silicon wafer at 1000^0 C.
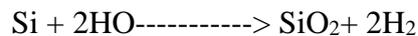
$$Si + 2HO\text{-----------}> SiO_2 + 2H_2$$

→ Silicon dioxide plays an important role in shielding of the surface so that dopant atoms, by diffusion or ion implantation, may be driven into other selected regions.

→ SiO2 is an extremely hard protective coating & is unaffected by almost all reagents except by hydrochloric acid. Thus it stands against any contamination.
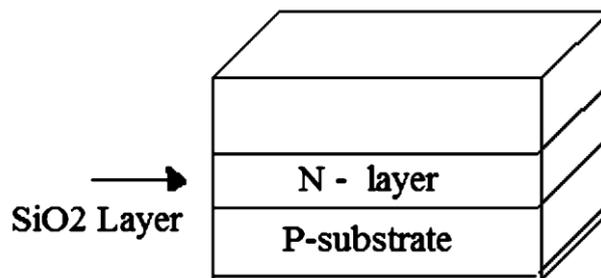
2.2.3 MASKING AND ETCHING

1. Explain the process of masking and photo-etching in IC fabrication. (Dec – 07) (7) (Dec – 14, 16) (6, 13)

Or

What is photolithography? What is the purpose of diffusion? (Dec – 13, 14) (8) [Apr/May 2019]

Or

Explain in detail about photo-lithography. (Dec – 03, 16) (May – 05) (4, 7)

Photolithography:

→ The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO₂ layer.

→ As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist).

→ The mask, a black and white negative of the required pattern, is placed over the structure.

→ When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes polymerized.

→ The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photo resist film.

Photoresist film 5000-10000Å

SiO₂ — Silicon wafer
(a)

Ultraviolet radiation

Photo mask

SiO₂ — Silicon wafer Photo resist
(b)

Polymerised photoresist

SiO₂ — Silicon wafer
(c)

Photoresist

SiO₂ — Silicon wafer
(d)
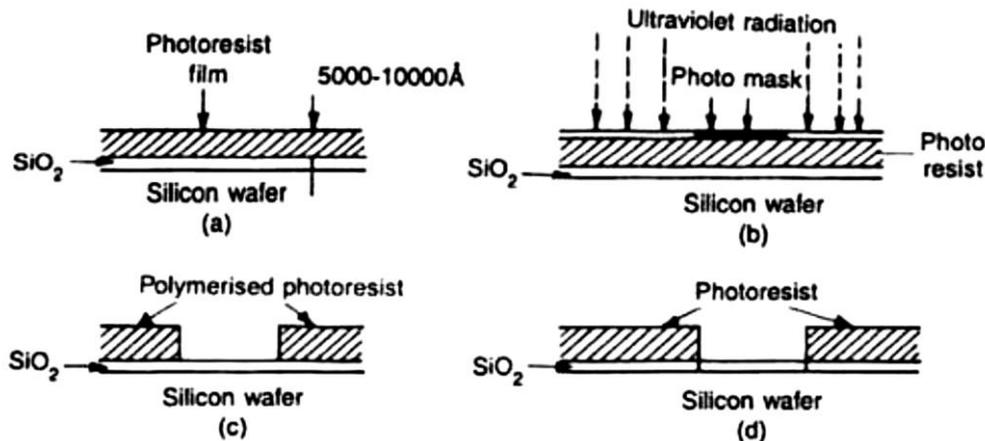
→ The polymerized region is cured so that it becomes resistant to corrosion.

→ Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photoresist.

→ This creates openings in the SiO_2 layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure.

→ After diffusion of impurities, the polymerized photoresist is removed with sulphuric acid and by a mechanical abrasion process.

2.2.4 DIFFUSION OF IMPURITIES

7. Explain in detail about diffusion process in IC fabrication. (Dec – 06) (8)

2.2.4.1 Isolation Diffusion:

→ The integrated circuit contains many devices.

→ Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

→ The most important techniques for isolation are:

       1. PN junction Isolation

       2. Dielectric Isolation

→ In PN junction isolation technique, the P+ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom.

→ This method generated N-type isolation regions surrounded by P-type moats.

→ If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

→ The individual components are fabricated inside these islands.

→ This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

→ In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation.

→ The isolation is both physical and electrical.

→ This method is very expensive due to additional processing steps needed and this is mostly used for fabricating IC's required for special application in military and aerospace.

→ The PN junction isolation diffusion method is shown in figure. The process takes place in a furnace using boron source.

→ The diffusion depth must be at least equal to the epitaxial thickness in order to obtain complete isolation.

→ Poor isolation results in device failures as all transistors might get shorted together.

→ The N-type island shown in figure forms the collector region of the NPN transistor.

→ The heavily doped P-type regions marked P+ are the isolation regions for the active and passive components that will be formed in the various N-type islands of the epitaxial layer.

2.2.4.2 Base diffusion:

→ Formation of the base is a critical step in the construction of a bipolar transistor.

→ The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer.

→ Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit.

→ The value of these resistors depends on the diffusion conditions and the width of the opening made during etching.

→ The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled.

→ The base sheet resistivity should be fairly high (200- 500Ω per square) so that the base does not inject carriers into the emitter.

→ For NPN transistor, the base is diffused in a furnace using a boron source.

→ The diffusion process is done in two steps, pre deposition of dopants at 900^0 C and driving them in at about 1200^0 C.

→ The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps.

→ Figure shows that P-type base region of the transistor diffused in the N-type island (collector region) using photolithography and isolation diffusion processes.

2.2.4.3 Emitter Diffusion:

→ Emitter Diffusion is the final step in the fabrication of the transistor.

→ The emitter opening must lie wholly within the base.

→ Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low resistivity ohmic contact path for the emitter terminal.

→ The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base.

→ A Phosphorus source is commonly used so that the diffusion time id shortened and the previous layers do not diffuse further.

→ The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth.

→ The active base is then a P-region between these two junctions which can be made very narrow by adjusting the emitter diffusion time.

→ Various diffusion and drive in cycles can be used to fabricate the emitter. The Resistivity of the emitter is usually not too critical.

→ The N-type emitter region of the transistor diffused into the P-type base region is shown below.

→ However, this is not needed to fabricate a resistor where the resistivity of the P-type base region itself will serve the purpose.

→ In this way, an NPN transistor and a resistor are fabricated simultaneously.

8. Explain in detail about ion implantation in IC fabrication. (Dec – 03) (6)

2.5. Ion implantation technique:

→ It is another technique to introduce impurities into a silicon wafer.

→ In this process silicon wafer are placed in a vacuum chamber, and are scanned by a beam of high energy ions. (boron for p- type, phosphorus for n- type)

→ These ions are accelerated by energies between 20 kV to 259 kV.

→ These ions strike the silicon wafers, they penetrate some distance into wafer.

→ The depth of any penetration of any particular type of ion increasing accelerating voltage.

→ It is performed at low temperature. Therefore, previously diffused regions have a lesser tendency for lateral spreading.

→ In diffusion process, temperature has to be controlled over a large area inside the oven, where as in ion implantation process, accelerating potential & beam content are dielectrically controlled from outside.
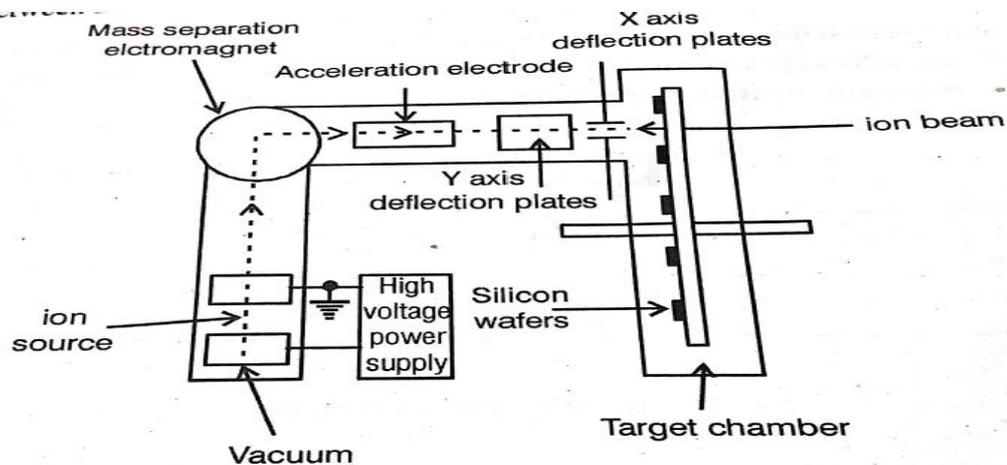
Fig 2.5 Ion implantation

2.5.1 Advantages of Ion Implantation:

1. Doping levels can be precisely controlled since the incident ion beam can be accurately measured as an electric current.

2. The depth of the dopant can be easily regulated by control of the incident ion velocity. It is capable of very shallow penetrations.

3. Extreme purity of the dopant is guaranteed.

4. The doping uniformity across the surface can be accurately controlled.

5. Because the ions enter the solid as a directed beam, there is very little spread of the beam, thus the doping area can be clearly defined.

6. Since this is a low-temperature process, the movement of impurities is minimized.

9. Explain the importance of isolation and discuss the different methods of isolation. (May – 07) (6)

Or

Describe in detail any two isolation techniques used to provide isolation between various components in IC fabrication with illustration. (May – 14) (16)

2.6. ISOLATION TECHNIQUES:

2.6.1 p-n junction isolation:

→ Consider a p-substrate with n-type epitaxial layer grown over it.

→ To provide isolation, a p-type impurity with high concentration is diffused selectively into an epitaxial layer such that it reaches to the p-substrate as shown below.

p-n junction isolation technique
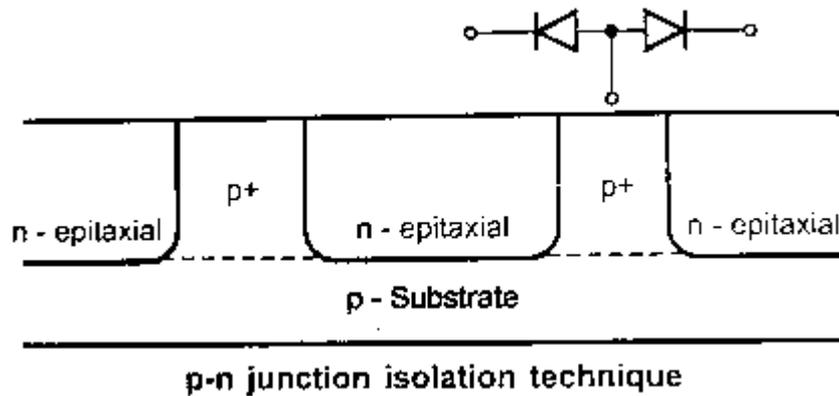
→ From the fig. it is clear that n-epitaxial region forms a region which is surrounded by p-type regions.
→ This region is called **island**.
→ Two regions are connected back-to-back and these two back-to-back diodes serve as **isolation regions** if both are reverse biased.
→ The main advantage of p-n junction isolation is that different components can be fabricated within the isolation islands.
→ But the disadvantage is the presence of undesirable and unavoidable parasitic capacitances at the islands.

2.6.2 Dielectric isolation:

→ In dielectric isolation, a layer of solid dielectric such as SiO_2 or ruby completely surrounds each components thereby producing isolation, both electrical & physical.

Dielectric isolation technique
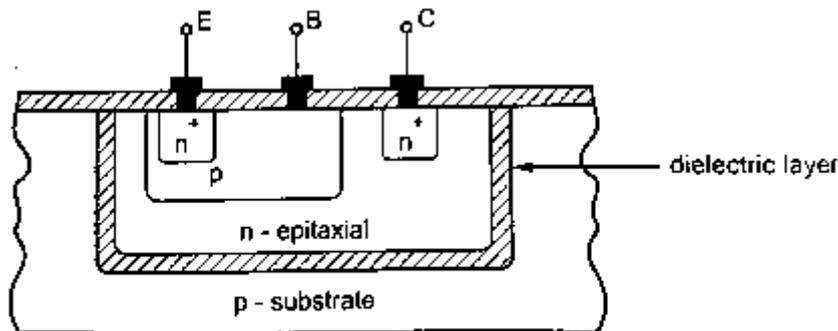
→ This isolating dielectric layer is thick enough so that its associated capacitance is negligible.
→ Also, it is possible to fabricate both pnp& npn transistors within the same silicon substrate which is the main advantage of this technique.
→ But the disadvantage is the increase in cost. As the technique requires additional steps in fabrication to deposit a dielectric layer, this technique is expensive.

2.7. CONTACT MASK:

→ After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals.
→ Heavily concentrated phosphorus N^+ dopant is diffused into these regions simultaneously.
→ The reason for the use of heavy N^+ diffusion is explained as follows:

> ➤ Aluminium, being a good conductor used for interconnection, is a P-type of impurity when used with silicon.

> ➤ Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped N^- material.

> ➤ Introducing a high concentration of N^+ dopant caused the Si lattice at the surface semi-metallic.

> ➤ Thus the N^+ layer makes a very good ohmic contact with the Aluminium layer. This is done by the oxidation, photolithography and isolation diffusion processes.

2.8. METALLIZATION:

$\rightarrow$ The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices.

$\rightarrow$ Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is 1μ m.

$\rightarrow$ Metallization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in figure.

$\rightarrow$ Metallization is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires.
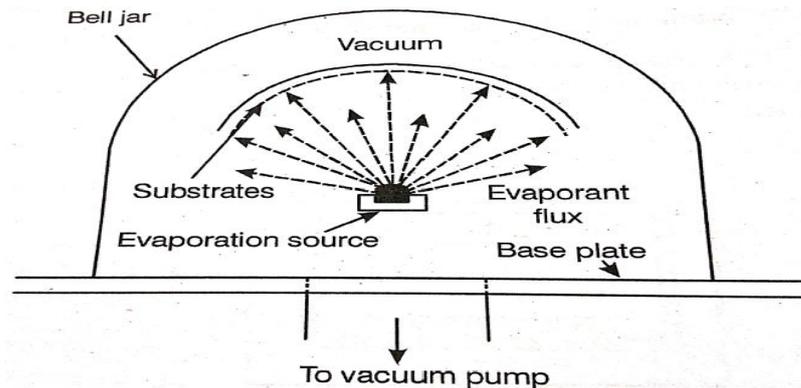
Fig 2.8: Metallization

2.9. PASSIVATION/ ASSEMBLY AND PACKAGING:

$\rightarrow$ Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device.

$\rightarrow$ This protects it against mechanical and chemical damage during subsequent processing steps.

$\rightarrow$ Doped or un doped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers.

$\rightarrow$ The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallization.

10. Completely describe the various stages involved in the fabrication of an R, C and transistor in a single chip. (May – 05) (16) [Apr/May 2019]

Or

Describe briefly the various stages involved in the fabrication of IC. Draw the layout of a circuit by considering an example. (May – 07, 17] [Dec – 07, 15) (13, 10, 8)

Or

With the help of neat diagram explain the steps involved in the fabrication of the circuit shown in the Fig. using IC technology. (May – 04) (16)
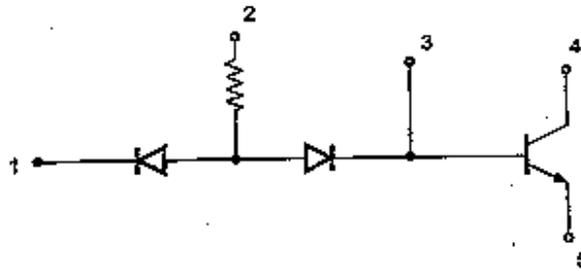
Or

With respect to BJT based circuit given below, explain the various steps to implement the circuit into a monolithic IC. (Dec – 14)(May-17, 18) (13, 10)
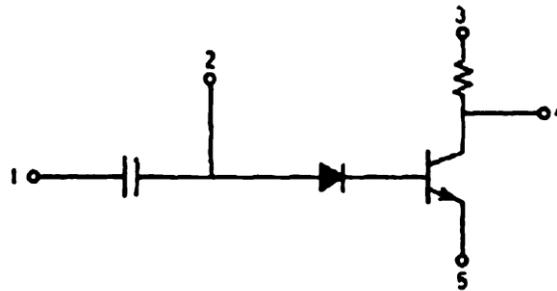
A. Preparation of Wafer:

→ The starting material for the integrated circuit is p-type silicon which is called substrate.

→ Typically the thickness of the wafer ranges between 400 µm to 500 µm.

→ The diameter of the silicon wafer ranges between 100 mm to 200 mm.

→ For the acceptor concentration of 1.4×10^{15} atoms/ cm^3 and the resistivity is $10 – 15$ Ω cm.

p-substrate   resistivity 10 - 15 Ω cm
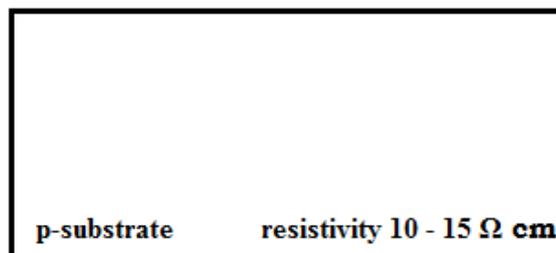
B. Epitaxial growth:

→ Generally the doping types of the substrate and the epitaxial layer are opposite to provide isolation.

→ Thus n-type epitaxial layer is grown on p-type substrate which has resistivity of the order $1 - 2$ Ω cm.

→ The epitaxial layer is useful as other components are fabricated within this layer.

→ This layer may act as an element of diode, diffused capacitor of collector of transistor.

n-epitaxial layer	$1 - 5\,\Omega$ cm
p-substrate	
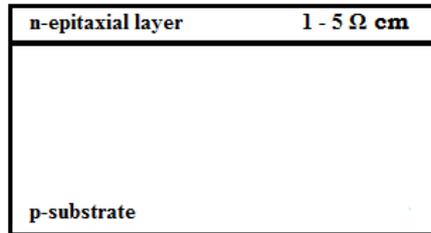
C. Oxidation:

→ After the growth of an epitaxial layer, SiO_2 layer is grown on then-epitaxial layer.

→ This oxide layer is grown by using thermal oxidation method.

→ The thickness of the SiO_2 layer is smaller as compared to previous layers.

→ Typically it ranges between 0.05 to 2 µm.

SiO₂ layer

n-epitaxial layer

p-substrate
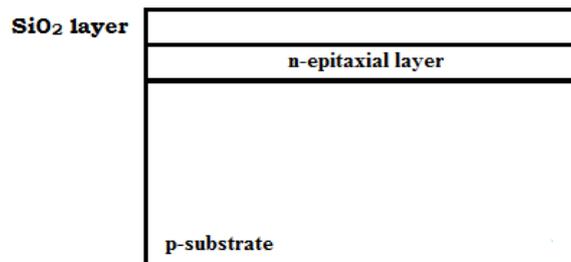
D. Lithographic process:

→ Then the wafer is coated with negative photoresist.

→ To isolate the components of the circuit, p + type layer is diffused.

→ For this a opening has to be made using the proper mask. So proper mask is kept on a wafer and then U.V. light is passed.

→ After that it is photo-etched to get a wafer with openings for isolation diffusion.

mask
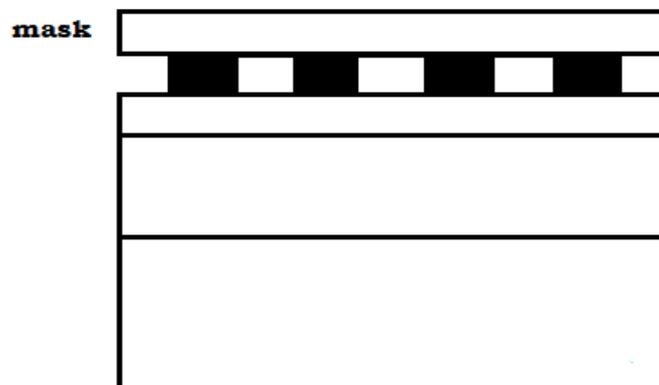
E. Isolation diffusion using p – n junction Isolation technique

21

$\rightarrow$ After the lithographic process, from the openings from where SiO_2 is etched out, heavy doping of p-type is diffused for very long interval such that the impurities reach p-substrate penetrating n-type epitaxial layer.

$\rightarrow$ Thus we get Isolation Island for four components.

$\rightarrow$ Generally the concentration of acceptor atoms between the Isolation Islands is kept higher than p-substrate which ensures perfect electrical isolation.
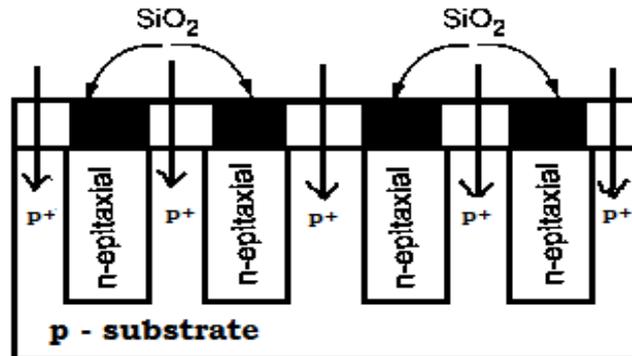
F. Base diffusion

$\rightarrow$ After isolation diffusion once again a layer of SiO_2 is grown over a wafer and then using lithographic technique different pattern is marked on wafer to have opening for the diffusion of p-type impurity such as boron.

$\rightarrow$ The impurity diffusion depth is controlled so that it cannot penetrate epitaxial layer to reach p-substrate.

$\rightarrow$ This serves as base of transistor, anode of diode etc.
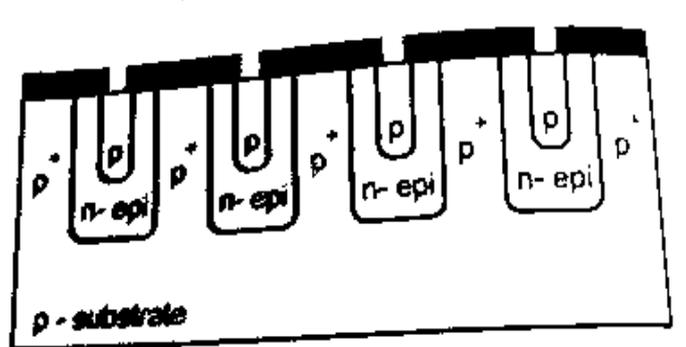
G. Emitter diffusion

$\rightarrow$ After base diffusion, another set of window is required to diffuse n-type impurity for the capacitor, diode and transistor.

$\rightarrow$ Hence again SiO_2 layer is grown on the wafer using different mask, new set of windows is opened using photo lithographic process.

$\rightarrow$ Then through the new set of windows, n-type impurity e.g. phosphorous is diffused which forms the emitter of transistor and cathode of diode.

$\rightarrow$ The windows are etched by using wet etching technique.
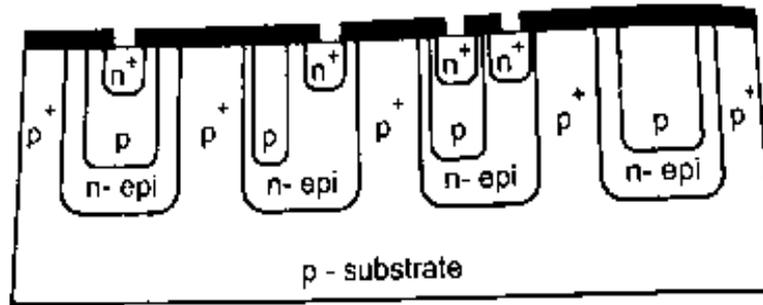
H. Metallization

→ The final step in the process of IC fabrication is making interconnection using aluminium metal.

→ For this again wafer is grown with SiO_2 layer and using new photo-mask, new set of windows is opened at points from where terminals are to be brought out.

→ After the interconnections are made IC is subjected to the packaging process.
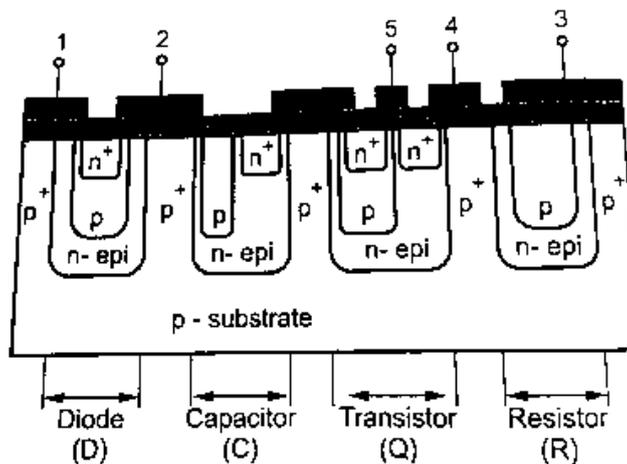
3. REALISATION OF MONOLITHIC IC'S AND PACKAGING

11. Briefly explain the various types of IC packages. Mention the criteria for selecting an IC package. (May-15) (Nov-17)(13, 8)

3.1 Packaging of ICs

→ After completing all the fabrication processes, several chips are ready on a wafer.

→ Each of the chips is nothing but a complete circuit. Now the next step is to separate out these chips and package them individually.

→ Using a diamond tipped tool, lines are scribed along the rectangular grids on the surface of the wafer.

→ The wafer is cut off along the lines drawn using the sharp diamond tipped tool.

→ Thus individual chips are separated from each other. Then each chip is assembled on a suitable package.

→ For comparing and assessing different packages, features are considered:

　　(i) Maximum pin count
　　(ii) Dimensions
　　(iii) Pitch (spacing between the centres of adjacent pins)
　　(iv) Encapsulating material (ceramic or plastic)

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(v) Mode of mounting (plated through hole - TH or surface mount - SM)

(vi) Maximum power dissipation.

$\rightarrow$ For TH mounting DIP (dual in line package) and PGA (pin grid array) are the only standard packages.

$\rightarrow$ For small scale integration (SSI) and medium scale integration (MSI),the different packages available are SIP (single in-line package), ZIP (zig-zag-in-line package) and QIPC (quad-in-line package) with TH mounting type.

$\rightarrow$ For low pin counts the packages available are SO (small out-line package), SSOP (Shrunk small out-line package). Both these are with SM mounting type.

$\rightarrow$ With SM mounting types there are two more packages namely chip carrier and TQFP(thin quad flat pack).

$\rightarrow$ The chip carrier uses either plastic or ceramic as encapsulating material. The TQFP has very low profile and small weight.

$\rightarrow$ The following table gives the different package types with their abbreviations.

Package Type	Abbreviation
Dual-in-line	DIP
Small outline	SO_1 SOIC
Shrunk small outline package	SSOP
Single-in-line	SIP
Zigzag-in-line	ZIP
Quad-in-line	QIP
Plastic leaded chip carrier	PLCC
Leadless ceramic chip carrier	LCCC
Leadless chip carrier	LLCC or LCC
Leaded chip carrier	LDCC
Flat pack	FP
Quad flat pack	QFP
Ceramic Quad flat pack	CQFP
Plastic Quad flat pack	PQFP
Thin Quad flat pack	TQFP
Pin grid array	PGA
Plastic Pin grid array	PPGA
Ceramic Pin grid array	CPGA

Package Type	Pin Count Range	Mounting type
Dual-in-line	8 – 64	TH
Single-in-line	5 – 40	TH
Zigzag-in-line	14 – 28	TH
Quad-in-line	14 – 64	TH
Small outline	8 – 32	SM
Chip Carrier	16 – 200	SM
Flat pack	10 – 300	SM
Pin grid array	68 – 500	SM

PGA

SOP

QFP

SSOP

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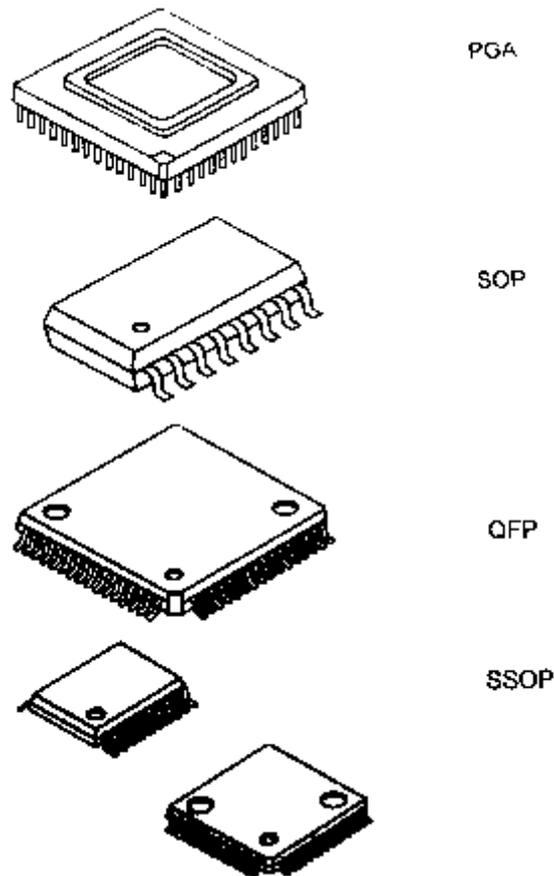
12. With neat sketches explain the fabrication of diodes and capacitors.

Or

Explain the various methods of fabricating diodes in monolithic integrated circuits. (Dec – 05, Dec – 03) (May-18) (10, 13, 16)

Or

Discuss briefly about the fabrication methods of diodes and transistors. (Dec – 13) (16)

Or

Discuss the different ways to fabricate diodes. (Dec – 07) (Dec – 14) (10)

Or

Explain in step-by-step basis the fabrication of planar p-n junction diode with illustrations. (May – 14) (8)

4. FABRICATION OF DIODES, CAPACITANCE, RESISTANCE, FETS AND PV CELL

4.1 Diode Fabrication:

→ Diodes are used extensively in the integrated circuits for various applications such as digital applications.

→ Note that in the integrated circuits, a p-n junction diode is formed from the bipolar transistor.

→ Generally any two terminals of the transistor are connected together to get one terminal of diode, while the remaining terminal of the transistor serves as the second terminal of diode.

→ Different transistor connections to utilize it as a diode are as shown in the Fig. below.

→ Depending upon desired circuit performance and application, diode connection is selected.

→ The diode represented in Fig. (a) is used in digital circuits for high speed applications because of its lowest storage time and lowest forward voltage drop.

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$\rightarrow$ The diodes represented in Fig. (b) and (e) are used as stored charged devices.

$\rightarrow$ The diodes represented in Fig. (c) and (d) have highest breakdown voltage.

(a)   (b)   (c)

(d)   (e)
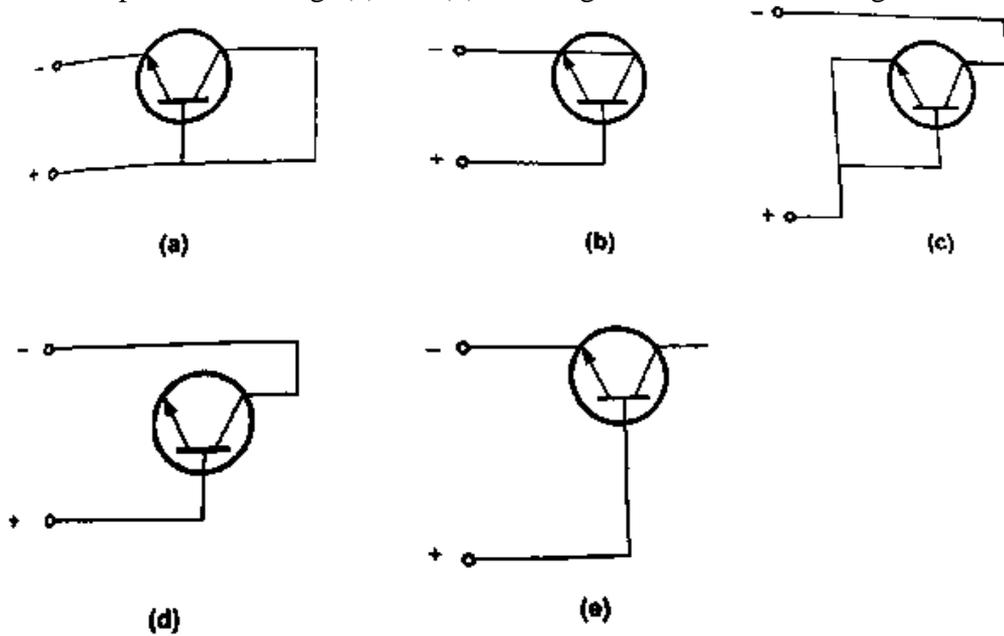
4.1.1 Fabrication of a planar p-n junction diode is illustrated as follows:

❖ The starting material for the planar p-n junction diode is n+ substrate which is grown by using Czochralski growing process. The substrate is about 150 µm thick.
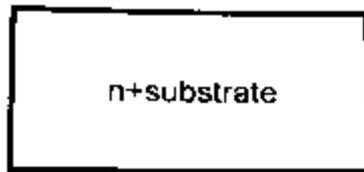
n+substrate

❖ Using epitaxial growth process, layer of n-type silicon is deposited on the substrate. The layer is about 1 to 5 µm thick.

n-epitaxial

n+substrate
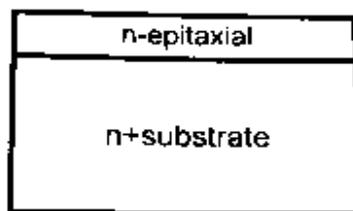
❖ Using oxidation process, Silicon dioxide (SiO_2) is deposited.

SiO_2

n-epitaxial

n+substrate
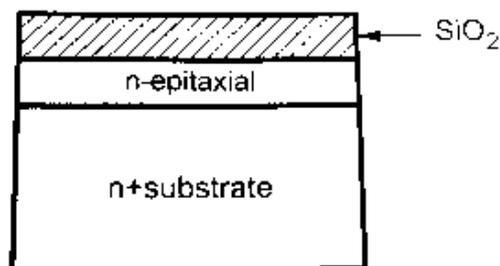
❖ The surface is then coated with positive photoresist.
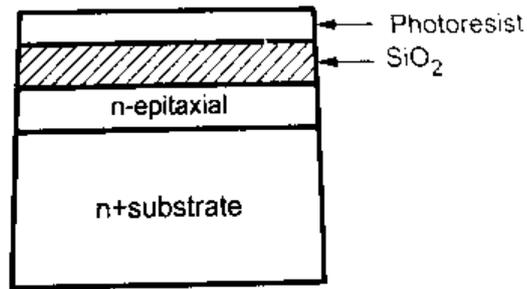
❖ Appropriate mask is placed over the positive photoresist layer. It is properly aligned and then exposed to the ultraviolet light.
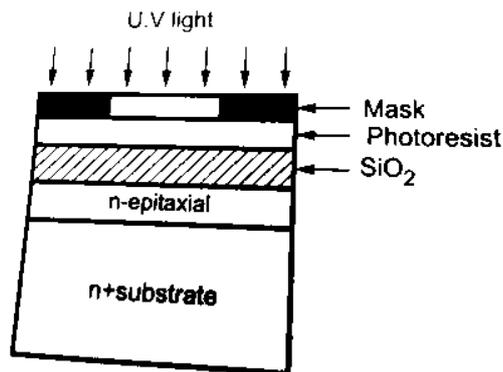
❖ Then the mask is removed and photoresist is removed. Using etching process, only silicon dioxide layer under the exposed resist is etched.
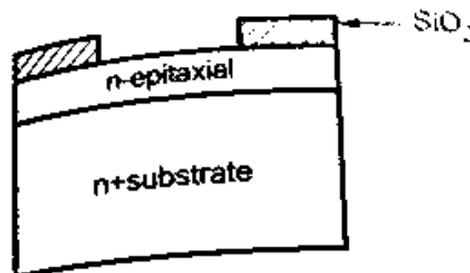
❖ Then to form p-region, boron is diffused using ion-implantation process.
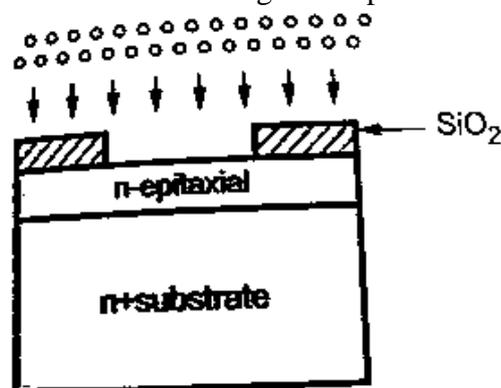
❖ Boron diffuses in silicon easily, but not in SiO_2. The resulting p-region is defined by the oxide opening. The Width of p-region is slightly greater than the oxide opening because of lateral doping during dopant diffusion.

SiO₂ — n-epitaxial / p / n+substrate
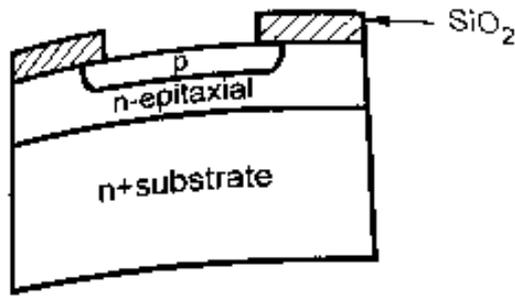
❖ Using Metallization, thin film of aluminium is deposited.

Aluminum film
SiO₂
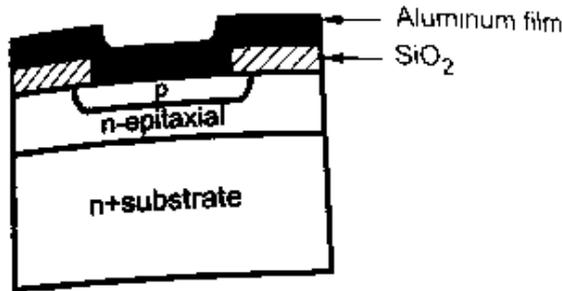
❖ Then the metalized area is covered with photoresist. Another mask is placed over photoresist which ensures areas of metal to be preserved.

Mask
Photoresist
Aluminum film
SiO₂
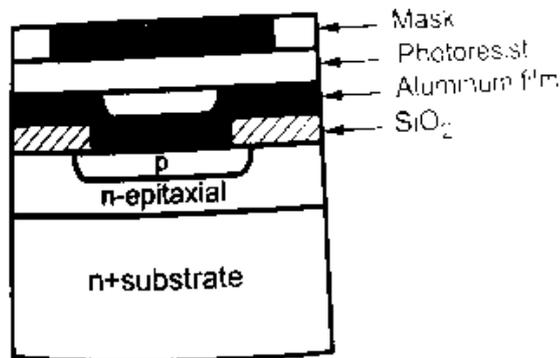
❖ The wafer is then etched to remove unwanted metal. The photoresist is then dissolved. The contact metal is deposited on the back surface and using heat treatment ohmic contacts are made.

SiO₂
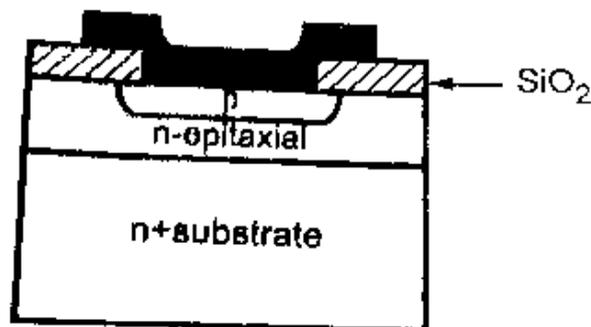
4.2 Capacitor Fabrication:

→ Monolithic capacitors are not frequently used in IC since they are limited in the range of values obtained and their performance.

→ Two common methods used for obtaining integrated capacitors are:

- Junction capacitor
- MOS and thin film capacitor

4.2.1 JUNCTION CAPACITOR

→ The capacitor is formed by reverse- biased junction j2 which separates the epitaxial n- type layer from the upper p- type diffusion area.

→ However parasitic capacitance c is inevitable due to the junction, j1 between n- type epitaxial layer and substrate. Also series resistance results due to bulk resistance of n- region.
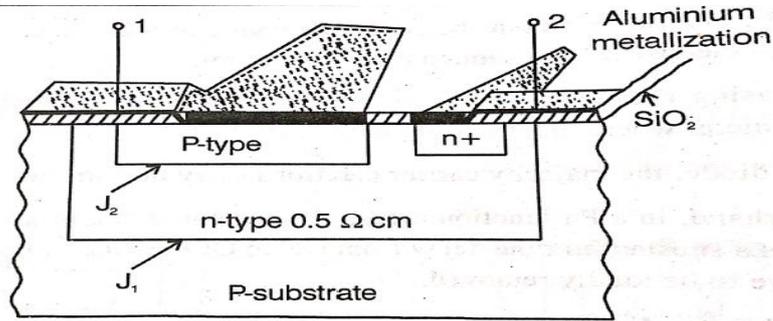
Fig 4.2.1 Junction capacitor

4.2.2 MOS AND THIN FILM CAPACITOR

→ It is basically a parallel plate capacitor with SiO_2 as dielectric.

→ The heavily doped n^+ region formed during emitter diffusion forms lower plate and thin film of aluminium metallization for upper plate of capacitor with SiO_2 as dielectric.
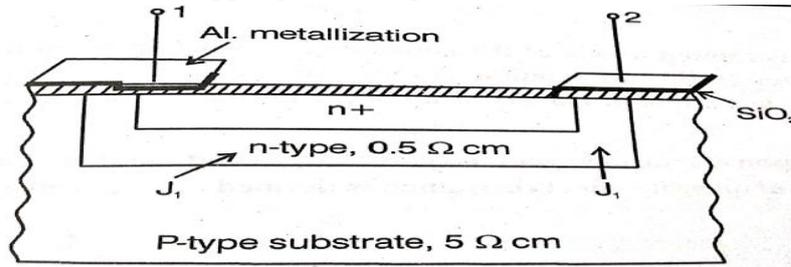
Fig 4.2.2 MOS capacitor

14. Explain the various methods used for fabricating IC resistors and compare their performance. (Dec – 14) (10)

Or

With neat sketches describe the various types of integrated resistors. (Dec – 07) (8)

Or

Discuss with neat diagram, the DC characteristics of OP- AMP with necessary expressions. (Nov/Dec 2019) (13)

4.3 FABRICATION OF RESISTORS

→ The resistors are grouped into two groups: one formed within monolithic and other composed of film resistors.

→ The monolithic IC resistors consists suitably dimensioned layers which would form part of the transistor normally.

→ Four different methods are available for fabricating integrated resistors namely:

- Diffused resistor
- Epitaxial resistor
- Pinched resistor
- Thin film resistor

4.3.1 Diffused resistor

→ If the resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion, then it is called **diffused resistor**.

→ It is very economical process as no additional steps in fabrication are needed.

→ But the limitation of the diffused resistor is that the range of the value of resistance is very small.

→ For larger value of resistor, the larger area of silicon is required.

→ Hence the high value resistances are realized by using pinch resistor as shown in the Fig.

→ The amount of silicon required for the value of resistor beyond 100 kΩ is relatively low.

→ The accuracy of such resistors is poor. For high value resistors accuracy is not important point to take care.

→ It consists of p base layer constricted by an n+ emitter layer, leading to an effective thickness equal to base thickness of an, PN transistor.
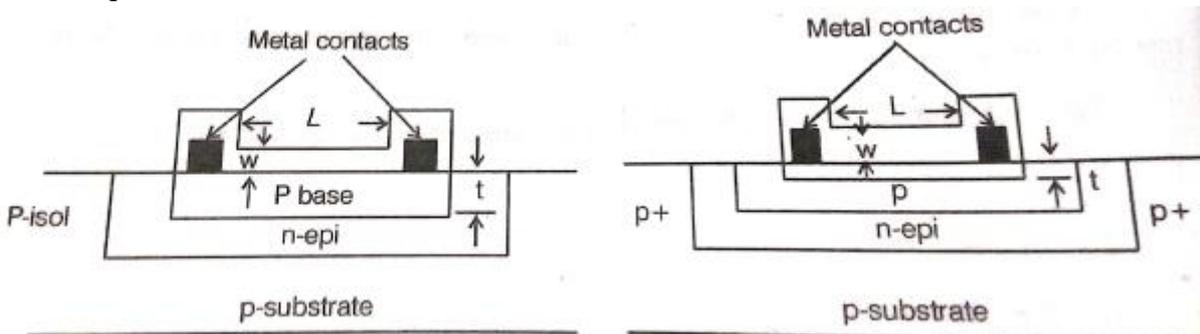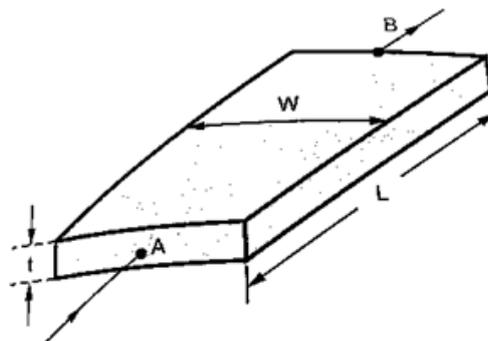

Fig 4.3.1 (a) Base resistor   Fig 4.3.1 (b) Emitter resistor

→ As we have already studied that the resistance can be realized by using a defined volume of semiconductor region, consider a sheet of material with length L and Width W as shown in the Fig. Let t be the thickness and ρ be the uniform resistivity and cross section area A=L*t.

Sheet resistor

→ The resistance R between layers A and B is given by,

$$R = \frac{\rho L}{A} = \frac{\rho L}{tW} \qquad (1)$$

→ For square surface area, W = L, then the resistance of the material is given by,

$$R_s = \frac{\rho L}{tL} = \frac{\rho}{t} \qquad (2)$$

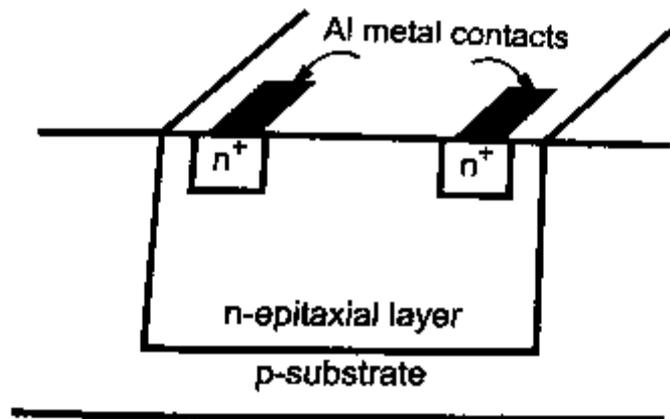→ Thus rearranging equation (1) using equation (2) we can write,

$$R = R_s \left(\frac{L}{W}\right) \qquad (3)$$

→ Here ratio $\left(\frac{L}{W}\right)$ is called **aspect ratio**.

→ Thus using this technique, base resistor in the range 20 Ω to 300 kΩ can be fabricated.

→ Similarly the resistance of the emitter diffusion can be fabricated as sheet resistor but the range of resistance is only 10 to 1 kΩ.

4.3.2 EPITAXIAL RESISTOR:

Epitaxial resistor

→ By using n-epitaxial collector layer, the large value resistances than base and emitter diffusion can be achieved.

→ Such resistors are called epitaxial resistors as shown in the Fig. above.

4.3.3 PINCHED RESISTOR

→ The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-sectional area.

→ In pinched resistor, this technique is used to achieve a high value of sheet resistance from the ordinary base diffused resistor.

→ It can offer resistance of the order of mega ohms in a smaller area.

→ In this structure no current can flow in the N- type material since the diode realized at contact 2 is biased in the reverse direction.

→ Only smaller reverse saturation current can flow in the N- region. Therefore by forming this N-region in the base diffusion, conduction path for the current has been reduced and pinched.

→ The resistance between the contact 1 , 2 increases as the width narrows down and hence it acts as a pinched resistor.
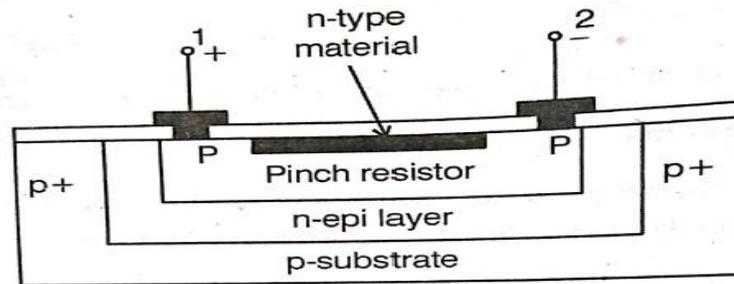
Fig 4.3.3 Pinched resistor

4.3.4 THIN FILM RESISTOR

→ In this a very thin metallic film usually of Nichrome (NiCr) of thickness less than 1 µm is vapour deposited on the SiO_2 layer.

→ Using masked etching, desired geometry of this thin film is achieved to obtained suitable values of resistors.

→ The ohmic contacts are made using A1 metallization and usual masked etching techniques Nichrome resistors are available with typical sheet resistance values of 40 to 400Ω/ square depending upon film thickness, so the resistance in the range of 20 to 50 kΩ can be obtained.
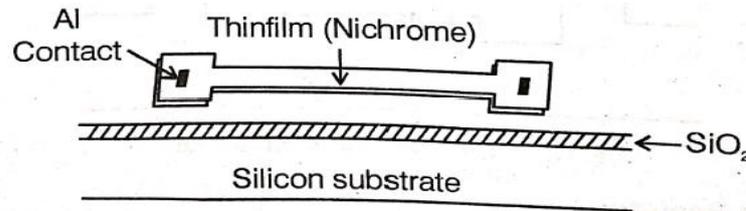
Fig 4.3.4 Thick film resistor

4.3.4.1 Advantages

→ They have lesser and small parasitic components and hence their high frequency behaviour is better.

→ The value of resistors can be easily adjusted even after fabrication by cutting a part of resistor with a laser beam.

→ They have low temperature coefficient, thereby making them stable.

4.3.4.2 Disadvantages

→ Additional steps required in their fabrication process.

15. Explain about MOSFET fabrication. Or explain the fabrication of FET in detail. [Apr/May 2019]

4.4 FABRICATION OF FET:

→ The FET is a device in which the flow of current through the conducting region is controlled by an electric field and hence the name Field Effect Transistor (FET).

→ Based on the construction, the FETs are classified into 2 types,

- Junction Field Effect Transistor (JFET)
- Metal Oxides Semiconductor Field Effect Transistor (MOSFET)

4.4.1 JFET Fabrication

→ The basic processes used are the same as in BJT fabrication.

→ The epitaxial layer which formed the collector of the BJT is used as n- Channel of JFET.

→ The p+ gate is formed in n- channel by the process of ion-implementation or diffusion.

→ The n+ regions have formed under the source and drain contact regions to provide ohmic contact.
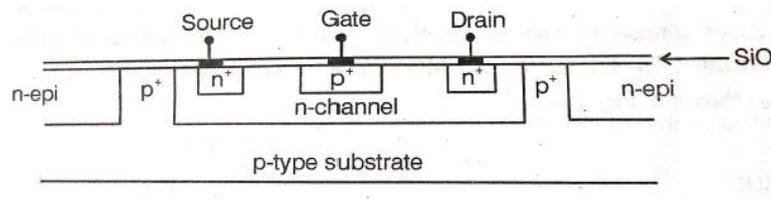

Fig 4.4.1 n- channel JFET

4.4.2 Integrated MOSFETs

→ MOSFETS are classified as follows:

(i) Enhancement mode MOSFET

ii) Depletion mode MOSFET

→ In MOSFETS gate terminal is isolated from the FET channel by silicon dioxide insulating layer.

→ As the layer is insulating type, it provides very high input resistance.

→ In providing superior barrier for impurities penetrating SiO_2 layer, silicon nitride (Si_3N_4) is sandwiched between two silicon dioxide (SiO_2) layers.

→ This helps in increasing overall dielectric constant.

→ The n-channel MOSFET of enhancement and depletion mode are as shown in the Fig. (a) and (b) respectively.
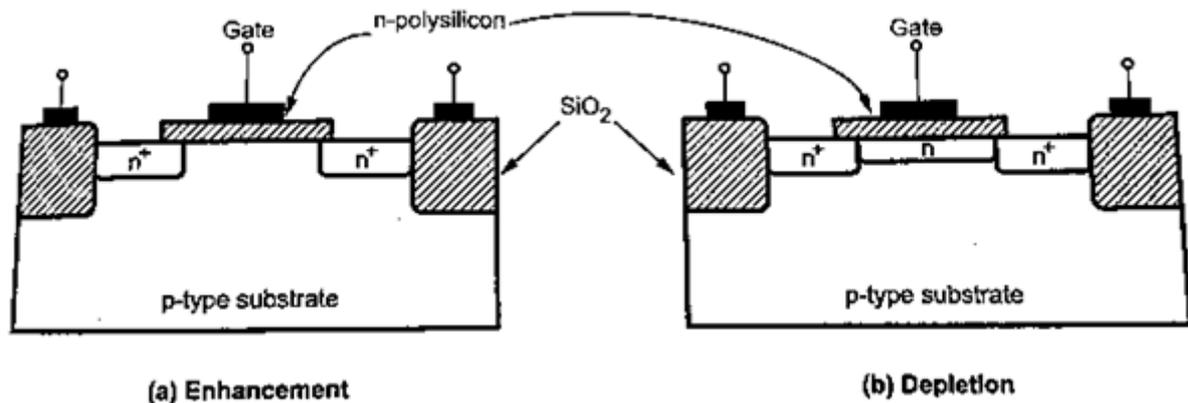

(a) Enhancement   (b) Depletion

Fig 4.4.2 n- channel MOSFET

→ In the enhancement mode MOSFET is in OFF state when gate-source bias is zero while MOSFET turns ON by positive gate source voltage.

→ In depletion mode, because of n-implanted channel, conduction is possible in ON state for zero gate source voltage, while negative gate source voltage is required to turn it OFF.

(ii) **Write a note on CMOS technology.**

Or

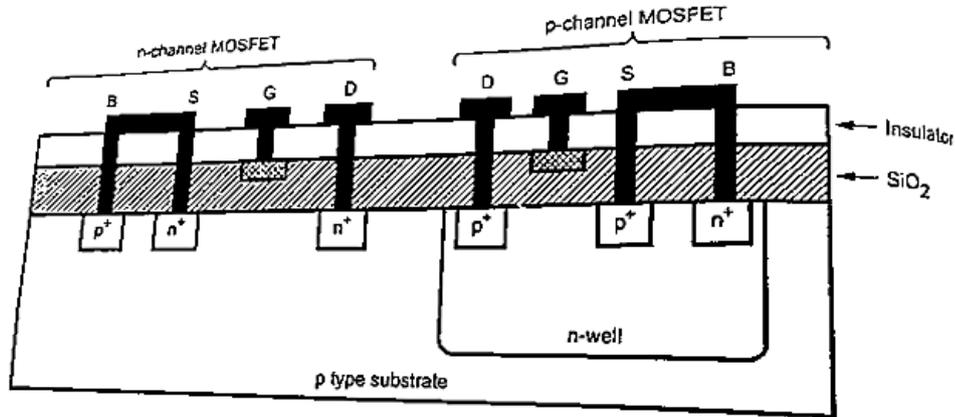**Explain CMOS fabrication with neat sketches. (Dec – 14) (May-18) (13, 8)**

4.4.3 FABRICATION OF CMOS:

→ When n-channel MOSFET and p-channel MOSFET both are integrated on same the device is chip, termed as complementary CMOS.

→ In CMOS fabrication, n –type well is diffused in p-type substrate.

→ Also p-channel MOSFET is fabricated within this n-well.

→ Basically this n-well forms substrate for p-channel MOSFET.

→ In the fabrication of p-channel MOSFET two additional steps are required as compared to n-channel MOSFET fabrication.

→ The additional steps are formation of n-well and ion-implantation of p-type source and drain regions.

→ The cross section of CMOS IC is as shown in the Fig.

Fig 4.4.3 CMOS process

4.5 FABRICATION OF PV CELL

→ A PV cell means photovoltaic cell or solar cell which works on photovoltaic effect. It generates voltage proportional to the light incident on it.

4.5.1 Steps of fabrication of PV cell

4.5.1.1 Refining silicon:

→ The available mineral in earth is SiO_2. This is used to obtain silicon by removing oxygen.

→ For this it is heated to 1500- 2000 °C in an electrode arc furnace with coal and charcoal i.e., reaction with carbon.

→ The silicon obtained is 98% pure which contains the impurities like iron, aluminium etc.

→ To remove these impurities, this silicon reacted with hydrous HCL to obtain $SiHCL_3$. Along with hydrogen at 1100 °C to produce pure silicon.

4.5.1.2
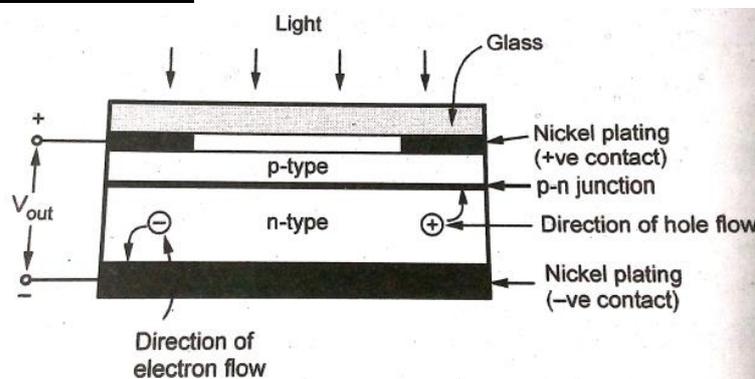### Screen printed PV cell fabrication

Fig 4.5 Construction

→ The first step in this process is to obtain silicon wafer of 10 x 10 sq.cm and 0.5 mm thick. It is then p- type doped so as to obtain p- type wafer.

→ The wafer is then heated in a furnace at 800- 1000°C with a phosphorous. This cause small amount of phosphorous to be deposited on the outer layer of silicon.

→ The phosphorous is required below the screen printed contact to maintain low contact resistance.

→ The wafers cut are then textured by etching pyramids on the wafer surface with a chemical solution. The texturing ensures better light travel inside the wafer by reducing reflection.

→ The cells are stacked one on the top of the other for removal of the junction at the edge of the wafer. The edges of the cells are etched by a highly reactive plasma gas to remove the junction.

→ Then the wafer is placed upside down and a screen is lowered onto the rear of the cell along with the metal paste. A full aluminium layer printed on the rear on the cell, with subsequent alloying through firing, produces back surface field.

→ This is done by placing the cell in a second furnace at a very high temperature. This firing process destroys the rear n- layer so that the aluminium makes contact with the p- type bulk.

→ The second print of aluminium is required for solderable contact. The cell is then flipped over for the printing on the front.

→ The front contact is printed in a similar manner as the rear contact. The finished cell is ready for encapsulation into a module.

→ An extra metal contact strip is soldered to the bus bar during the encapsulation to lower the cell series resistance.

→ The square shape of a multi crystalline substrate simplifies the packing of cells into a module.

CHARACTERISTICS OF OP-AMP

Ideal OP-AMP characteristics - DC characteristics - AC characteristics - differential amplifier – frequencyresponse of OP-AMP - Basic applications of OP-AMP - Inverting and Non-inverting Amplifiers, summer, differentiator and integrator V/I & I/Vconverters.

Part – A – 2 Mark Questions

1. List out the ideal characteristics of OP-AMP. (May – 03, 05, 09, Dec – 06, 15, Nov/Dec 2019)

    i. Infinite voltage gain

    ii. Infinite input impedance

    iii. Zero output impedance

    iv. Infinite bandwidth

    v. Infinite CMRR

    vi. Infinite Slew Rate

    vii. Zero PSRR

2. Define CMRR of an amp. (May –04, 15, Dec – 05, 09, 10)

$\rightarrow$ CMRR means Common Mode Rejection Ratio.

$\rightarrow$ The ability of the differential amplifier to reject common mode signals is expressed by the ratio of differential gain to common mode gain which is called its Common Mode Rejection Ratio (CMRR).

$\rightarrow$ It is defined as the ratio of differential voltage gain $A_d$to common mode voltage gainA_c.

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$$

$\rightarrow$ Ideally the common mode voltage gain is zero and hence the ideal value of CMRR is infinite.

3. Define slew rate. What causes it? (May – 03, 04, 08, Dec – 11)

$\rightarrow$ The maximum rate of change of output voltage with respect to time is called slew rate of the op-amp.

$\rightarrow$ It is expressed as,$S = \left.\frac{dV_0}{dt}\right|_{max}$ and measured in V/µsec.

$\rightarrow$ The slew rate is caused due to limited charging rate of the compensating capacitor and current limiting and saturation of the internal stages of an op-amp, when high frequency large amplitude signal is applied. The slew rate equation is, $S = 2\pi f V_m$ (V/sec).

4. List the methods used to provide the external frequency compensation. [APR/MAY2019]

$\rightarrow$ The methods used to provide external frequency compensation are:

    i. Dominant pole compensation

    ii. Pole-Zero compensation

    iii. Feed-Forward compensation

5. Mention some of linear applications of OP-AMP. (Dec – 05)

$\rightarrow$ Some of the linear applications of op-amp are:

    i. Inverting Amplifier

    ii. Non-Inverting Amplifier

    iii. Voltage Follower

    iv. Integrator

    v. Differentiator

    vi. Instrumentation Amplifier

6. What is PSRR? What should be its ideal value? (May – 03)

→ PSRR is power supply rejection ratio. It is defined as the change in the input offset voltage due to the change in one of the two supply voltages when other voltage is maintained constant.

→ It's ideal value should be zero.

7. What are the merits and demerits of Dominant pole compensation method?

Merits:

    i. As the noise frequency components are outside the smaller bandwidth, the noise immunity of the system improves.

    ii. Adjusting value of f_d, adequate phase margin and the stability

Demerits:

    i. The only disadvantage of the method is that the bandwidth reduces drastically.

8. What happens when the common terminal of V+ and V- sources is not grounded?

→ If the common point of the two supplies is not grounded, twice the supply voltage will get applied and it may damage the op-amp.

9. What is meant by differential amplifier?

→ The differential amplifier is one which amplifies the difference between its two input signals.

→ The gain with which it amplifies the difference is called its differential gain and ideally it should be infinite.

10. What is frequency compensation?

→ The method of modifying loop gain frequency response of the op-amp so that it behaves like single break frequency response which provides sufficient positive phase margin is called **frequency compensation technique**.

11. Design an amplifier with a gain of -10 and input resistance of 10k.

Since the gain of the amplifier is negative, an inverting amplifier has been made.

Given that $R_1 = 10 \text{ k}\Omega$

Therefore, $R_f = - A_{CL} R_1$

$$= - (-10) \times 10 \text{ k}\Omega$$

$$= \mathbf{100 \text{ k}\Omega}$$

12. An input of 3V is fed to the non-inverting terminal of an op-amp. The amplifier has a R_i of 10KΩ and R_f of 10KΩ .Find the output voltage.
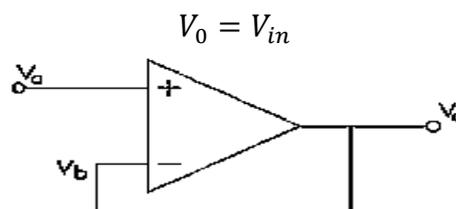
For a non-inverting amplifier,

$$A_f = 1 + \frac{R_f}{R_i} = 1 + \frac{10}{10} = 2$$

And $\quad A_f = \frac{V_0}{V_{in}} \quad$ where, $\quad V_{in} = 3V$

$$\therefore \quad V_0 = A_f V_{in} = 2 \times 3 = \mathbf{6V}$$

13. What is voltage follower? (Dec – 09)

→ A circuit in which the output voltage (V_0) follows the input voltage (V_{in}) is called voltage follower circuit.

$$V_0 = V_{in}$$

**14. In practical op-amps, what is the effect of high frequency on its performance?**

→ The open-loop gain of op-amp decreases at higher frequencies due to the presence of parasitic capacitance.

→ The closed-loop gain increases at higher frequencies and leads to instability.

15. What is an op-amp? (Dec – 05)

→ The operational amplifier is basically an excellent high gain differential amplifier.

→ It amplifies the difference between its two inputs.

→ Due to its use in performing mathematical operations it has been given a name operational amplifier.

16. What is a precision diode? Draw the Circuit diagram of a half wave precision rectifier with waveform. (May – 03)

→ The major limitation of ordinary diode is that it cannot rectify voltages below the cut – in voltage of the diode.

→ A circuit designed by placing a diode in the feedback loop of an op – amp is called the precision diode and it is capable of rectifying input signals of the order of milli volt.

Positive precision half wave rectifier   Negative precision half wave rectifier
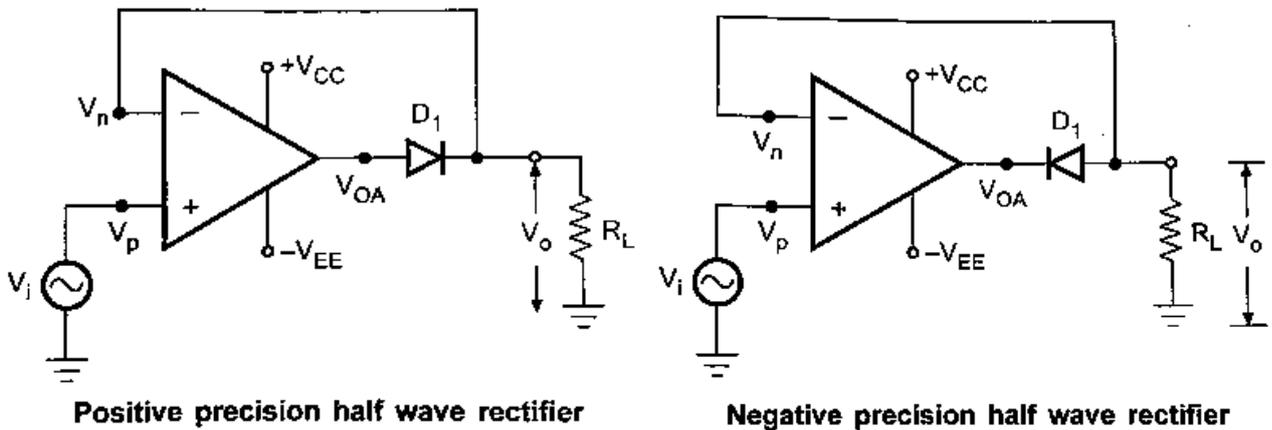
17. Draw the circuit diagram of an op-amp integrator. Give its output equation and mention its applications. (May – 04, 09, Dec – 06, 08)



Op-amp Integrator
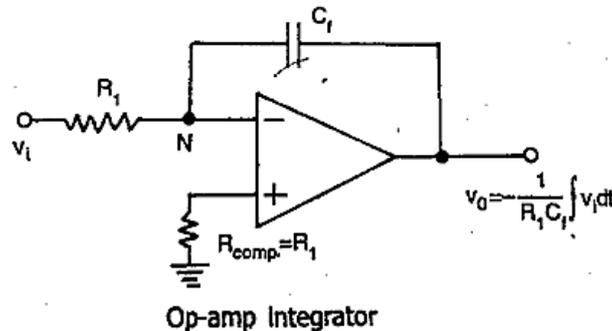
Its output is given by,

$$v_0(t) = -\frac{1}{R_1 C_f} \int_0^t v_i(t) \cdot dt + v_0(0)$$

The integrator circuits are most commonly used in the following applications:

1. In analog computers
2. In solving differential equations

3

3. In analog to digital converters
4. Various wave shaping circuits
5. In Ramp Generators

18. Draw the circuit diagram of differentiator using Op-amp. Write the expression for its output. (Dec – 09, May – 10, 17)

Op-amp differentiator
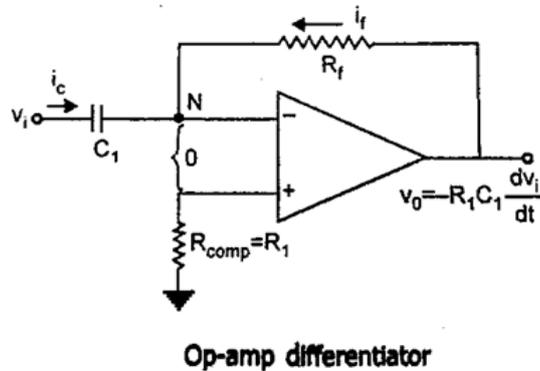
Its output expression is,

$$v_0 = -R_f C_1 \frac{dv_i}{dt}$$

19. The two input bias currents of an Op-amp are 22µA and 26 µA. What is the value of input offset current? Input bias current?

Given:

$I_{b1} = 22 \ \mu A$

$I_{b2} = 26 \mu A$

Solution:

The input offset current is given by,

$$I_{ios} = |I_{b1}| - |I_{b2}|$$
$$I_{ios} = |22 - 26|\mu A$$
$$\boldsymbol{I_{ios} = 4\mu A}$$

The input bias current is given by,

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$
$$\boldsymbol{I_b = \frac{22 + 26}{2} = 24\mu A}$$

20. Why IC 741 is not used for high frequency applications?

→ IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies.

→ As frequency increases the output gets distorted due to limited slew rate.

21. Mention some of the non – linear applications of op-amps. (Dec – 05)

→ Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti –log amplifier, multiplier are some of the non – linear op-amp circuits.

22. What is the need for frequency compensation in practical op-amp? (Dec – 10)

→ Frequency compensate on is needed when large bandwidth and lower closed loop gain is desired.

→ Compensating networks are used to control the phase shift and hence to improve the stability.

23. Define input offset voltage. (Dec – 07, May – 09, 15)

→ A small voltage applied to the input terminals to make the output voltages zero when the two input terminals are grounded is called input offset voltage.

24. Define input offset current. (Dec – 07, May – 09, 15) State the reasons for the offset currents at the input of the op-amp.

→ The base currents of the transistors used in the input stage of the differential amplifier are practically finite and the two currents differ in magnitude as perfect matched transistors are not possible in practice.

→ These currents are responsible for the input bias current and input offset current of an op-amp.

→ The difference between the bias currents at the input terminals of the op-amp is called as input offset current.

$$I_{ios} = |I_{b1}| - |I_{b2}|$$

25. Define Thermal Drift.

→ The dependence of the op-amp parameters on the temperature is indicated by a factor called temperature drift.

→ The change in the op-amp parameter corresponding to the change in the temperature is defined as the thermal drift of that parameter.

→ Thus $\frac{\Delta V_{ios}}{\Delta T}$ is called the input offset voltage temperature drift.

26. What is input bias current? (Dec – 07, May – 09)

→ The base currents of the transistors used in the input stage of the differential amplifier are practically finite and the two currents differ in magnitude as perfect matched transistors are not possible in practice.

→ These currents are responsible for the input bias current and input offset current of an op-amp.

→ The input bias current is the average of the two base currents I_{b1} and I_{b2}.

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$

27. Draw the circuit of a non-inverting amplifier and state the expression for its gain. (May – 08)
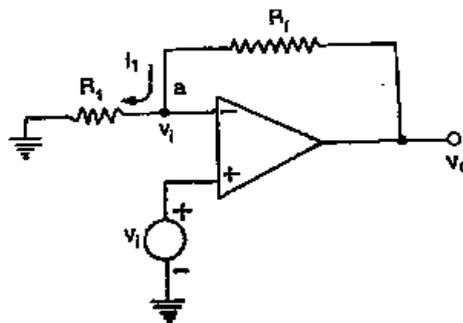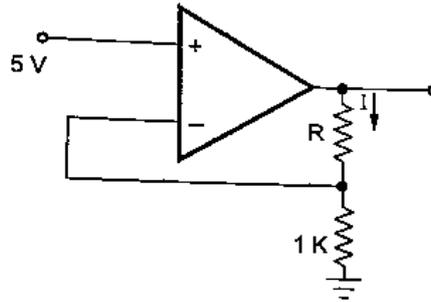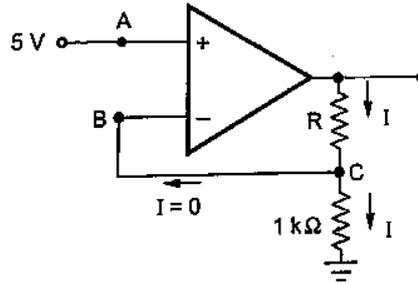

Non-Inverting amplifier

The gain of a non-inverting amplifier is given as,

$$Gain = 1 + \frac{R_f}{R_1}$$

28. Calculate the current I in the circuit shown. (May – 07)

Solution:

Due to virtual ground,

$$V_B = V_A = 5V$$

and $\qquad V_C = V_B = 5V$

As op-amp input current is zero, current through 1 kΩ is I.

$$\therefore I = \frac{V_C}{R} = \frac{5}{1 \times 10^3} = 5\ mA$$

29. Compare inverting and non-inverting amplifiers. (Dec – 10)

S. No	Inverting Amplifier	Non-Inverting Amplifier
1.	Voltage Gain = - R_f / R_1	Voltage Gain = 1 + R_f / R_1
2.	The output is inverted with respect to input.	No phase shift between input and output.
3.	The voltage gain can be adjusted as greater than, equal to or less than one.	The voltage gain is always greater than one.
4.	The input impedance is R_1.	The input impedance is extremely large.

30. How to obtain the average circuit from the inverting summer? (Dec – 09)

→ In an inverting summer if the values of resistances are selected such that $R_1 = R_2 = R$ and $R_f = R/2$ then the output is the average of the two inputs applied to the circuit.

31. Draw the circuit diagram of a practical integrator circuit. (Dec – 06)

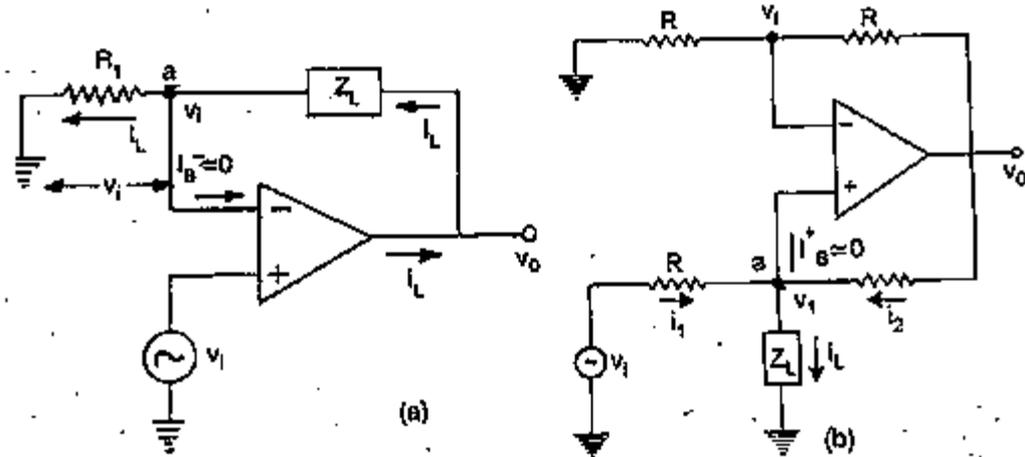Practical or lossy Integrator circuit

6
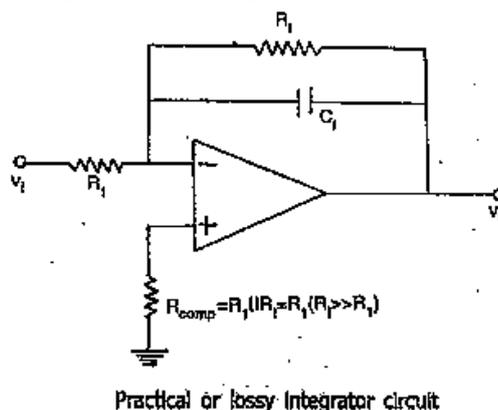
32. What is a V-I converter? (Dec – 08)

→ The circuit in which the output load current is proportional to the input voltage is called V to I converter.
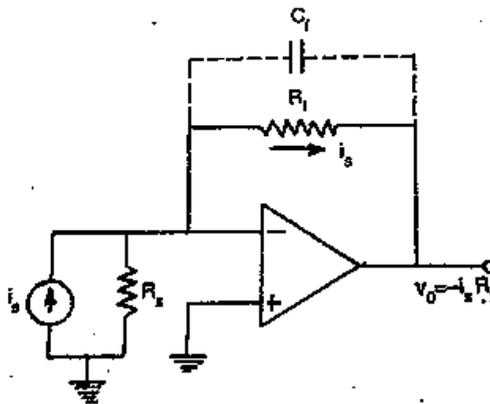
→ Mathematically it is given by, $I_L \propto V_{in}$.

33. Draw the circuit of op-amp based V-I converter. (May – 10)

Voltage to current converter with (a) floating load (b) grounded load

34. Draw the circuit of op-amp based I-V converter. (Dec – 10)

Current to voltage converter

35. Why integrators are preferred over differentiators in analog computers? (May – 09, Dec – 11)

→ Integrators are preferred in analog computers because,

- o Gain of the integrators decreases as frequency increases hence easy to stabilize with respect to spurious oscillations. Gain of the differentiator increases with frequency.
- o The input impedance of integrator is constant. While that of differentiator decreases with frequency. So at high frequency it becomes very low and differentiator may get overloaded.
- o The differentiator has a tendency to amplify noise and drifts which may cause oscillations.
- o It is very easy to introduce initial voltages in case of integrators rather than differentiators.

35. Compare the ideal and practical op-amp characteristics. (May-18)

Ideal OPAMP	Practical OPAMP
Infinite voltage gain, so that it can amplify input signals of any amplitude.	Voltage gain is not infinite, but typically 10^5 to 10^8, so it is not able to amplify input signals smaller than 100 uV.
Infinite input resistance, so that almost any signal source can drive it and there is no loading of preceding stage.	Input resistance is typically 10^6 to 10^12 ohm (for FET input Op-Amps such as uAF771), so still it draws some current and not all source can drive it.
Zero output resistance, so that output can drive an infinite number of other devices.	Output resistance is typically 75 ohm for standard Op-Amps, so it has limit to deliver current to output devices.
Zero output voltage when input voltage is zero.	It is not able to give zero at output when input is zero, due to mismatching of input transistors.

36. How the op-amp can be used as a voltage follower circuit? (May-18)

Voltage Follower is simply a circuit in which output follows the input, means output voltage remains same as input voltage. It is also commonly known as Unity gain Op-amp Amplifier or Op-amp Buffer**.**

37. The O/P voltage of a certain OP-amp circuit changes by 20v in 4ms. What is its slew rate? [APR/MAY 2019]

$S = 2\pi f V_m$ m/s

T=4ms

F=1/T=1/4ms

$S = 2\pi \times 1/4ms \times 20v = 314$ m/s

38. Distinguish between input offset voltage and input offset current. Nov/Dec 2019.

  Input offset voltage
  → A small voltage applied to the input terminals to make the output voltages zero when the two input terminals are grounded is called input offset voltage.

  Input offset current
  → The difference between the bias currents at the input terminals of the op-amp is called as input offset current.

## 1. IDEAL OP-AMP CHARACTERISTICS

Part – B – 16Mark Questions

1.1 OPERATIONAL AMPLIFIER:

→ The operational amplifier, most commonly referred as 'op-amp' was introduced in 1940s. The first operational amplifier was designed in 1948 using vacuum tubes.

→ In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. Due to its use in performing mathematical operations it has been given a name operational amplifier.

→ Due to the use of vacuum tubes, the early op-amps were bulky, power consuming and expensive.

→ Robert J. Widlar at Fairchild brought out the popular 741 integrated circuit (IC) op-amp between 1964 and 1968.

→ The IC version of op-amp uses BITS and FETs which are fabricated along with the other supporting components, on a single semiconductor chip or wafer which is of a pinhead size.

→ With the help of IC op-amp, the circuit design becomes very simple. The variety of useful circuits can be built without the necessity of knowing about the complex internal circuitry.

→ Moreover, IC op-amps are inexpensive, take up less space and consume less power.

→ The IC op-amp has become an integral part of almost every electronic circuit which uses linear integrated circuit.

→ The modern linear IC op-amp works at lower voltages. It is so low in cost that millions are now in use annually.

Key Point: Because of their low cost, small size, versatility, flexibility and dependability, op-amps are used in the fields of process control, communications, computers, power and signal sources, displays and measuring systems. The op-amp is basically an excellent high gain d.c. amplifier.

Symbol:

The symbol for an op-amp along with its various terminals is as follows:


Op-amp symbol
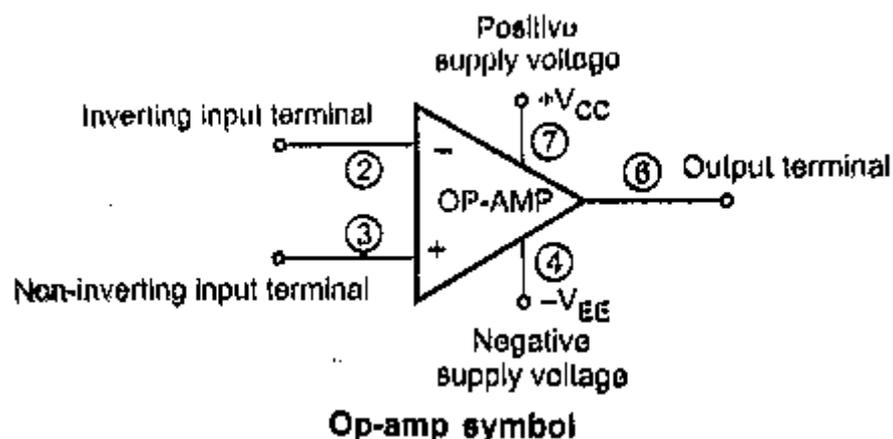
→ The op-amp is indicated basically by a triangle which points in the direction of the signal flow.
All the op-amps have at least following five terminals:

❖ The positive supply voltage terminal V_{CC} or $+ V$.

❖ The negative supply voltage terminal $- V_{EE}$ or V.

❖ The output terminal.

❖ The inverting input terminal, marked as negative.

❖ The non-inverting input terminal, marked as positive.

→ The input at inverting input terminal results in opposite polarity (antiphase) output.

→ While the input at non-inverting input terminal results in the same polarity (phase) output.

→ This is shown in the Fig. (a) and (b). The input and output are in antiphase means having 180° phase difference in between them while in-phase input and output means having 0° phase difference in between them.
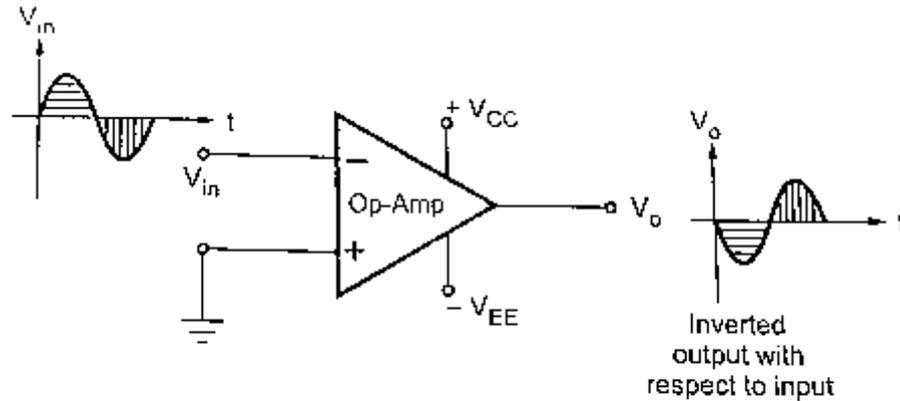

(a) Input applied to inverting terminal
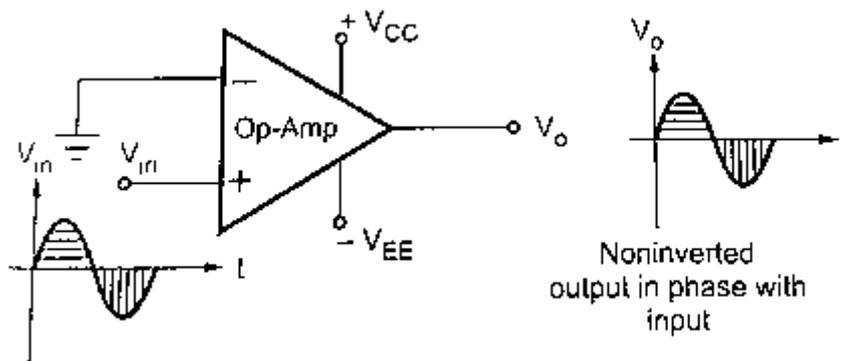
(b) Input applied to non - inverting terminal

1. Draw the Schematic block diagram of the basic OP-AMP.

1.2 BLOCK DIAGRAM REPRESENTATION OF OP-AMP:

→ As mentioned earlier, now-a-days op-amps are available in an integrated Circuit form.

→ Commercial integrated circuit op-amps usually consist of four cascaded blocks. The block diagram of IC op-amp is shown in the Fig.
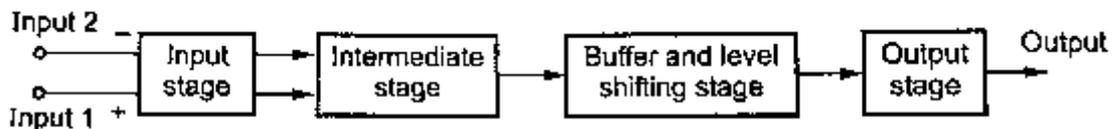
Internal block schematic of an op-amp

1.2.1 Input Stage:

→ The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals.

→ It also requires low output impedance. All such requirements are achieved by using the **dual input, balanced output differential amplifier** as the input stage.

→ The function of a differential amplifier is to amplify the difference between the two input signals.

→ The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier.
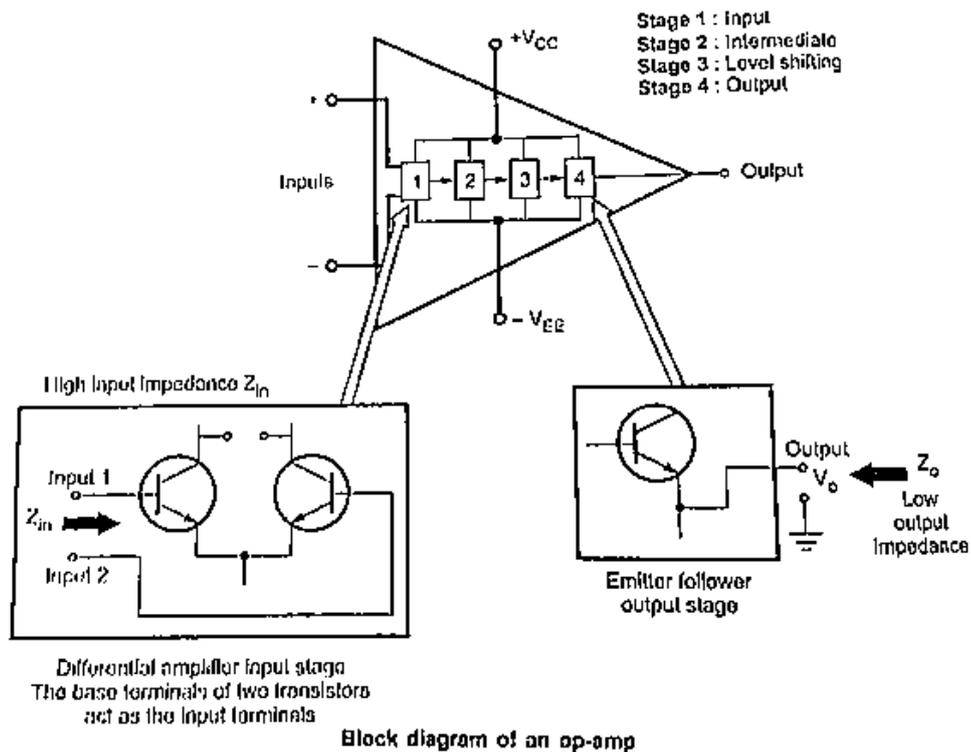
1.2.2 Intermediate Stage:

→ The output of the input stage drives the next stage which is an intermediate stage.

→ This is another differential amplifier with dual input, unbalanced i.e. single ended output.

→ The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain.

→ The main function of the intermediate stage is to provide an additional voltage gain required.

→ Practically, the intermediate stage is not a single amplifier but the chain of cascaded amplifiers called **multistage amplifiers**.

1.2.3 Level Shifting Stage:

→ All the stages are directly coupled to each other.

→ As the op-amp amplifies d.c. signals also, the coupling capacitors are not used to cascade the stages.

→ Hence the d.c. quiescent voltage level of previous stage gets applied as the input to the next stage.

→ Hence stage by stage d.c. level increases well above ground potential. Such a high d.c. voltage level may drive the transistor into saturation.

→ This further may cause distortion in the output due to clipping.

→ This may limit the maximum a.c. output voltage swing without any distortion.

→ Hence before the output stage, it is necessary to bring such a high d.c. voltage level to zero volts with respect to ground.

→ The **level shifter** stage brings the d.c. level down to ground potential, when no signal is applied at the input terminals.

→ Then the signal is given to the last stage which is the output stage.

→ The buffer is usually an emitter follower whose input impedance is very high. This prevents loading of the high gain stage.

1.2.4 Output Stage:

→ The basic requirements of an output stage are low output impedance, large a.c. output voltage swing and high current sourcing and sinking capability.

→ The **push-pull complementary amplifier** meets all these requirements and hence used as an output stage.

→ This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground.

→ The stage raises the current supplying capability of the op-amp. In short, the overall block diagram can be shown as in the Fig.

Stage 1 : Input
Stage 2 : Intermediate
Stage 3 : Level shifting
Stage 4 : Output

Block diagram of an op-amp

1.2.5 Currents and Impedances:

→ Practically an input stage is a transistorised differential amplifier stage using the two transistors.

→ The base terminals of these two transistors are the two input terminals of the op-amp.

→ Some small d.c. base current is necessary to maintain the operating state of the transistors.

→ These two base currents are the input bias currents of the op-amp. Typically the d.c. input current is of the order of 500 nA or less.

→ The input impedance Z_{in} is very high of the order of 1 MΩ or greater.

→ To increase the input impedance field effect transistors (FETs) are used instead of bipolar junction transistors (BJTs).

→ In such a case, gates of the two FETs are the input terminals of the op-amp.

→ The output stage is an emitter follower having very low output impedance.

→ The output impedance Z_0 is usually 75 Ω and the maximum output current is of the order of 25 mA.

1.3 IDEAL OP-AMP CHARACTERISTICS:

2. Explain various characteristics of ideal op-amp. Distinguish between ideal and practical characteristics. (12)

The Fig. shows an ideal op-amp. It has two input signals V_1 and V_2 applied to non-inverting and inverting terminals, respectively.

Ideal op-amp

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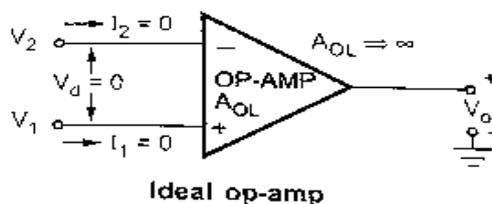
The following things can be observed for the ideal op-amp:

i. An ideal op-amp draws no current at both the input terminals i.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage.

ii. The gain of an ideal op-amp is infinite (∞), hence the differential output $V_d = V_1 - V_2$ is essentially zero for the finite output voltage V_0.

iii. The output voltage V_0 is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits.

These properties are expressed generally as the characteristics of an ideal op-amp. The various characteristics of an ideal op-amp are:

1. <u>Infinite voltage gain : ($A_{OL} = \infty$)</u>

It is denoted as A_{OL}. It is the differential open loop gain and is infinite for an ideal op-amp.

2. <u>Infinite input impedance : ($R_{in} = \infty$)</u>

The input impedance is denoted as R_{in} and is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

3. <u>Zero output impedance : ($R_0 = 0$)</u>

The output impedance is denoted as R_0 and is zero for an ideal op-amp. This ensures that the output voltage of the op-amp remains same, irrespective of the value of the load resistance connected.

4. <u>Zero offset voltage : ($V_{ios} = 0$)</u>

The presence of the small output voltage though $V_1 = V_2 = 0$ is called an offset voltage. It is zero for an ideal op-amp. This ensures zero output for zero input signal voltage.

5. <u>Infinite bandwidth :</u>

$\rightarrow$ The range of frequency over which the amplifier performance is satisfactory is called its **bandwidth**.

$\rightarrow$ The bandwidth of an ideal op-amp is infinite.

$\rightarrow$ This means the operating frequency range is from 0 to ∞. This ensures that the gain of the op-amp will be constant over the frequency range from d.c. (zero frequency) to infinite frequency.

$\rightarrow$ So op-amp can amplify d.c. as well as a.c. signals.

6. <u>Infinite CMRR : ($\rho = \infty$)</u>

The ratio of differential gain and common mode gain is defined as CMRR. Thus infinite CMRR of an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

7. <u>Infinite slew rate : ($S = \infty$)</u>

$\rightarrow$ This ensures that the changes in the output voltage occur simultaneously with the changes in the input voltage.

$\rightarrow$ The slew rate is important parameter of op-amp. When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes.

$\rightarrow$ If output does not change with the same rate as input then there occurs distortion in the output.

$\rightarrow$ Such a distortion is not desirable.

$\rightarrow$ **Infinite slew rate indicates that output changes simultaneously with the changes in the input voltage**.

$\rightarrow$ The parameter slew rate is actually defined as the maximum rate of change of output voltage with time and expressed in V /μs.

$$Slew\ rate = S = \left.\frac{dV_0}{dt}\right|_{max}$$

It's ideal value is infinite for the op-amp.

8. No effect of temperature:

The characteristics of op-amp do not change with temperature.

9. Power Supply Rejection Ratio: (PSRR = 0)

$\rightarrow$ he power supply rejection ratio is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant.

$\rightarrow$ It is also called **power supply sensitivity**.

$\rightarrow$ So if V_{CC} is constant and due to change in V_{CC}, there is change in input offset voltage then PSRR is expressed as,

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{CC}}\right|_{V_{EE}}\ constant$$

For a fixed V_{CC}, if there is change in V_{EE} causing change in input offset voltage then,

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{V_{EE}}\ constant$$

It is expressed in mV/V or μV/V and its ideal value is zero.

These ideal characteristics of op-amp are summarized as follows:

Characteristics	Symbol	Values
Open loop voltage gain	A_{OL}	∞
Input Impedance	R_{in}	∞
Output Impedance	R_0	0
Offset Voltage	V_{oo}	0
Bandwidth	B.W.	∞
C.M.R.R	P	∞
Slew Rate	S	∞
Power Supply Rejection Ratio	PSRR	0

1.4 PRACTICAL OP-AMP CHARACTERISTICS:

$\rightarrow$ The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amps.

$\rightarrow$ But basically the practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

$\rightarrow$ The important d.c. characteristics of op-amp are, 1. Input bias current (I_b), 2. Input offset current (I_{ios}) 3. Input offset voltage (V_{ios}), 4. Thermal drift

$\rightarrow$ The various characteristics of a practical op-amp can be described as below.

a) Open loop gain:

$\rightarrow$ It is the voltage gain of the op-amp when no feedback is applied practically it is several thousands.

b) Input impedance:

$\rightarrow$ It is finite and typically greater than 1 MΩ. But using FETs to; the input stage, it can be increased till several hundred MΩ.

c) Output impedance:

→ It is typically few hundred ohms. With the help of negative feedback, it can be reduced to a very small value like 1 or 2 ohms.

d) Bandwidth:

→ The bandwidth of practical op-amp in open loop configuration is very small. By application of negative feedback, it can be increased to a desired value.
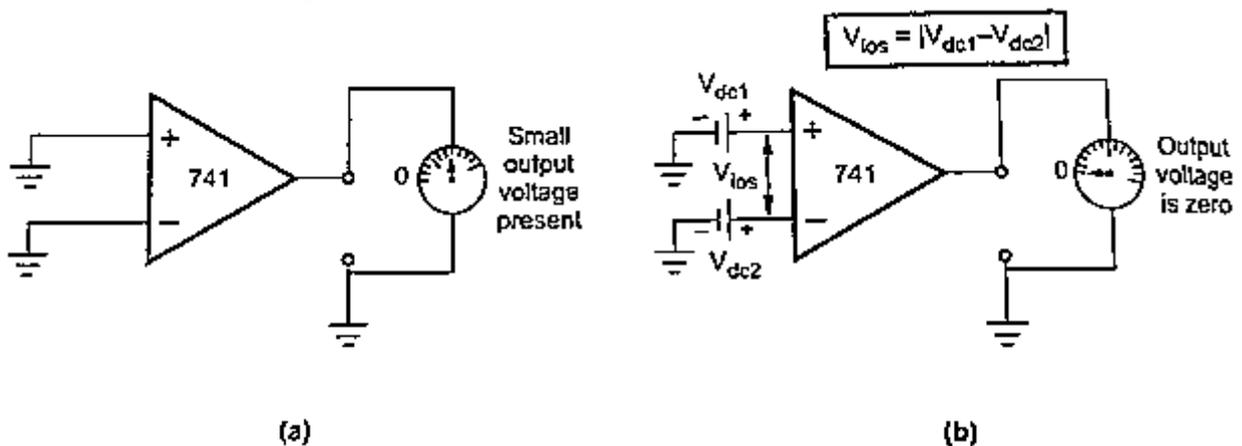
e) Input offset voltage:

→ Whenever both the input terminals of the op-amp are grounded, ideally, the output voltage should be zero.

→ However, in this condition, the practical op-amp shows a small non zero output voltage.

→ To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals.

→ Such a voltage makes the output exactly zero. This d.c. voltage, which makes the output voltage zero, when the other terminal is grounded is called **input offset voltage** denoted as V_{ios}.

→ The input offset voltage depends on the temperature. The concept of input offset voltage is shown in the Fig.
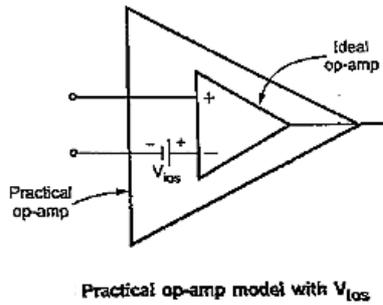

Concept of input offset voltage

→ The V_{ios} can be positive or negative hence absolute value of the V_{ios} is mentioned in the data sheet.
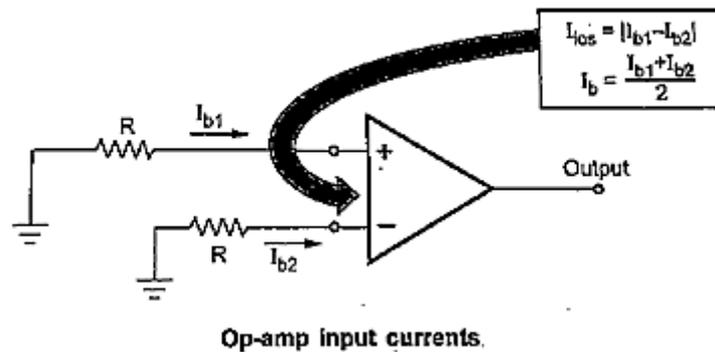
→ The smaller the value of V_{ios} better is the matching of the input terminals. The input offset voltage depends on the temperature.

→ Much time voltage to one of the input terminals is applied with the proper polarity so as to null the output, keeping other input terminal grounded. For ideal op-amp, V_{ios} is zero, hence practical Op-amp model is generally shown as in the Fig. with the indication of the input offset voltage. For op-amp 741 IC the input offset voltage is 6 mV.

Practical op-amp model with V_{ios}

f) Input bias current:

→ The average value of the two currents flowing into the op-amp input terminals is called **input bias current** and denoted as I_b. It is shown in the Fig.

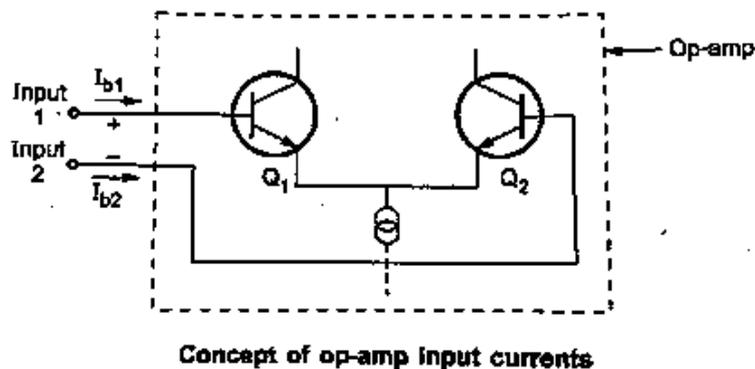**Op-amp input currents.**

Mathematically it is expressed as,

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

Ideally it should be zero while for op-amp 741 IC, maximum value of I_b is 500 nA.

Key Point: Both I_{ios} and I_b are temperature dependent.

g) Input offset current:

→ It is seen that the input stage of the op-amp is the dual input differential amplifier and the input terminals are the base terminals of the two transistors as shown in the Fig.

→ Hence the input currents of op-amp are the base currents of the two transistors Q_1 and Q_2 used in the input stage. Ideally, Q_1 and Q_2 must be perfectly matched and two base currents must be equal.

→ But practically the two input base currents differ by small amount.

Concept of op-amp input currents

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→ The algebraic difference between the currents flowing into the two input terminals of the op-amp is called **input offset current** and denoted as I_{ios}.

→ Mathematically it is expressed as,

$$I_{ios} = |I_{b1}| - |I_{b2}|$$

Where I_{b1} = Current entering into non-inverting input terminal

I_{b2} = Current entering into inverting input terminal

→ Ideally I_{ios} is zero while for op-amp 741 IC; maximum value of I_{ios} is 200 nA.

→ This current is responsible to produce the output though input terminals are grounded.

2. D.C. CHARACTERISTICS OF OP-AMP

| |
|---|
| **3. Explain the following terms in an OP-AMP. (Nov-17)** |
| ✓ **Bias current (4)**
✓ **Input offset current (4)**
✓ **Input offset voltage (4)**
✓ **Thermal drift (4)**

Or

Explain various DC and AC characteristics of an op-amp. Distinguish between ideal and practical characteristics. (12)

Or

Discuss in detail about the d.c. characteristics of an op-amp. (Dec – 14) (Nov/ Dec 2019) (13) |

2. D. C. CHARACTERISTICS OF OP-AMP:

→ The important d. c. characteristics of op-amp are,

      i. Input bias current (I_b)

      ii. Input offset current (I_{ios})

      iii. Input offset voltage (V_{ios})

      iv. Thermal drift

2.1 Input bias current:

→ The average value of the two currents flowing into the op-amp input terminals is called **input bias current** and denoted as I_b. It is shown in the Fig.
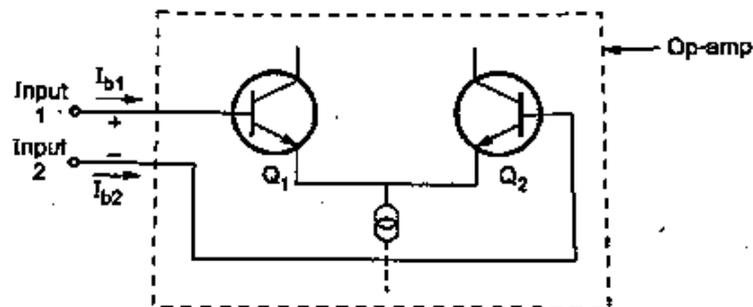

Op-amp input currents.
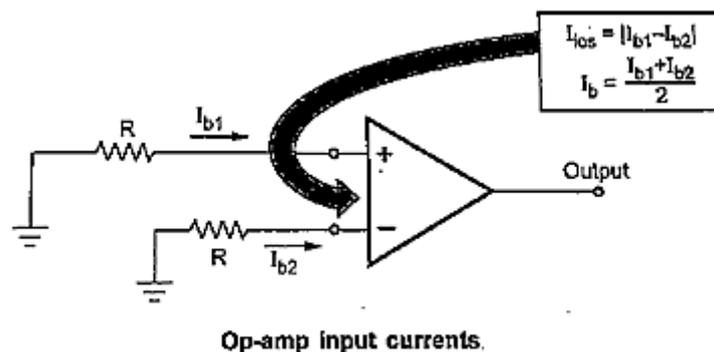
→ Mathematically it is expressed as,

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

→ Ideally it should be zero while for op-amp 741 IC, maximum value of I_b is 500 nA.

→ **Key Point:** Both I_{ios} and I_b are temperature dependent.

→ The effect of these parameters is to add the error to the expected d. c. output voltage. These parameters produce **output offset voltage** V_{oos}.

2.2 Input offset current:

→ It is seen that the input stage of the op-amp is the dual input differential amplifier and the input terminals are the base terminals of the two transistors as shown in the Fig.

→ Hence the input currents of op-amp are the base currents of the two transistors Q_1 and Q_2 used in the input stage.

→ Ideally, Q_1 and Q_2 must be perfectly matched and two base currents must be equal. But practically the two input base currents differ by small amount.

Concept of op-amp input currents

→ The algebraic difference between the currents flowing into the two input terminals of the op-amp is called **input offset current** and denoted as I_{ios}.

→ Mathematically it is expressed as,
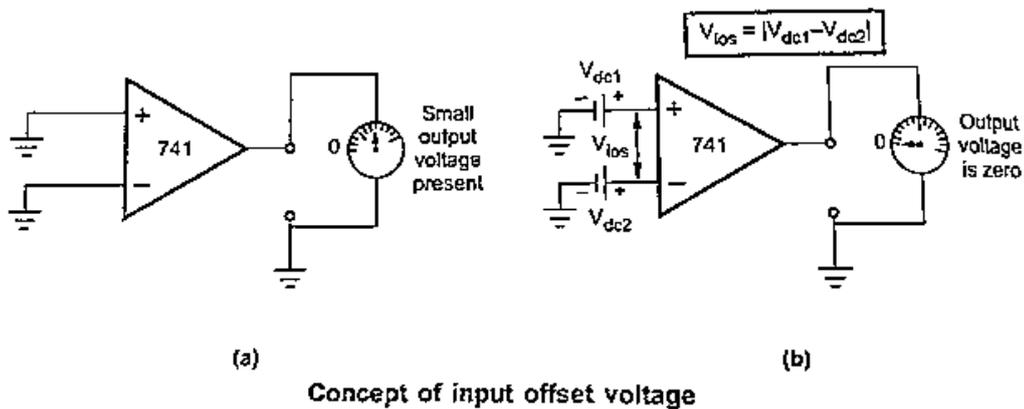
$$I_{ios} = |I_{b1}| - |I_{b2}|$$

Where I_{b1} = Current entering into non-inverting input terminal

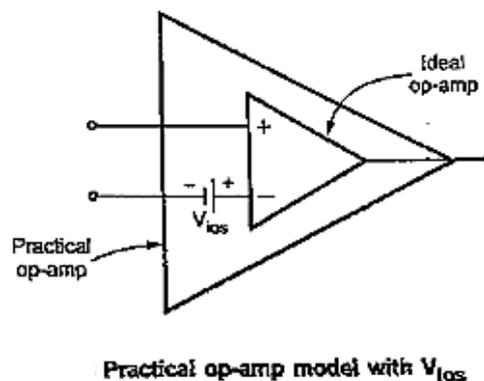I_{b2} = Current entering into inverting input terminal

→ Ideally I_{ios} is zero while for op-amp 741 IC, maximum value of I_{ios} is 200 nA. This current is responsible to produce the output though input terminals are grounded.

2.3 Input offset voltage:

→ Whenever both the input terminals of the op-amp are grounded, ideally, the output voltage should be zero.

→ However, in this condition, the practical op-amp shows a small non zero output voltage.

→ To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals.

→ Such a voltage makes the output exactly zero.

→ This d.c. voltage, which makes the output voltage zero, when the other terminal is grounded is called **input offset voltage** denoted as V_{ios}.

→ The input offset voltage depends on the temperature. The concept of input offset voltage is shown in the Fig.

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$$V_{ios} = |V_{dc1} - V_{dc2}|$$

Concept of input offset voltage

→ The V_{ios} can be positive or negative hence absolute value of the V_{ios} is mentioned in the data sheet.

→ The smaller the value of V_{ios} better is the matching of the input terminals.

→ The input offset voltage depends on the temperature.

→ Much time voltage to one of the input terminals is applied with the proper polarity so as to null the output, keeping other input terminal grounded.

→ For ideal op-amp, V_{ios} is zero, hence practical Op-amp model is generally shown as in the Fig. with the indication of the input offset voltage. For op-amp 741 IC the input offset voltage is 6 mV.

Practical op-amp model with V_{ios}

2.4 **Thermal Drift:**

→ The op-amp parameters input offset voltage V_{ios}, input bias current I_b and input offset current I_{ios} are not constants but vary with the factors:

    ❖ Temperature

    ❖ Supply voltage changes

    ❖ Time

→ The effect of change in temperature on the parameters is most severe.
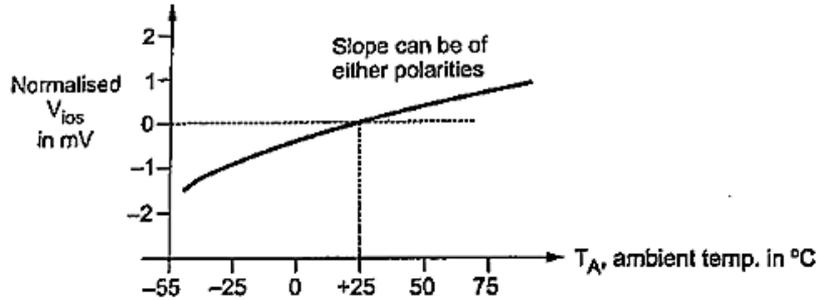
2.5 **Effect on Input Offset Voltage:**

→ The effect of change in temperature on the input offset voltage is defined by a factor called **thermal voltage drift**. It is also called as input offset voltage drift.

→ The thermal voltage drift is defined as average rate of change of input offset voltage per unit change in temperature. Mathematically it is given by,

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

Where, ΔV_{ios} = change in input offset voltage

$$\Delta T = \text{change in temperature}$$

$\rightarrow$ It is expressed in $\mu V/°C$. The drift is not constant and it is not uniform over specified operating temperature range.

$\rightarrow$ The value of the input offset voltage may increase or decrease with the increasing temperature.

$\rightarrow$ The Fig. shows the graph of normalized values of input offset voltage versus temperature, for MC 741 op-amp.

Input offset voltage drift

$\rightarrow$ The input offset voltage is zero at room temperature of 25°C. Referring to the graph shown in the Fig. the thermal voltage drift values can be obtained.

2.6 Effect on Input Offset and Bias Currents:

$\rightarrow$ Similar to the input offset voltage, input bias current and input offset current are not constants but vary with temperature.

$\rightarrow$ The effect of temperature on input bias current is defined by a factor called **input bias current drift** while effect on input offset current is defined by a factor called **input offset current drift**.

$\rightarrow$ The average rate of change of input bias current per unit change in temperature is called input bias current drift.

$\rightarrow$ The average rate of input offset current per unit change in temperature is called input offset current drift.

$\rightarrow$ Mathematically these drifts are given by,

$$\text{Thermal drift in input bias current} = \frac{\Delta I_b}{\Delta T}$$
$$\text{Thermal drift in input offset current} = \frac{\Delta I_{ios}}{\Delta T}$$

$\rightarrow$ Both the drifts are measured in $nA/^0C$ or $pA/^0C$. These parameters vary randomly with temperature i.e. they may be positive in one temperature range and negative in another.

$\rightarrow$ The Fig. shows the graph of normalized values of input bias current and input offset current versus temperature, for MC1741 op-amp.

$\rightarrow$ These curves are different for different types of op-amps and are generally provided by the manufacturers.

Input bias current drift
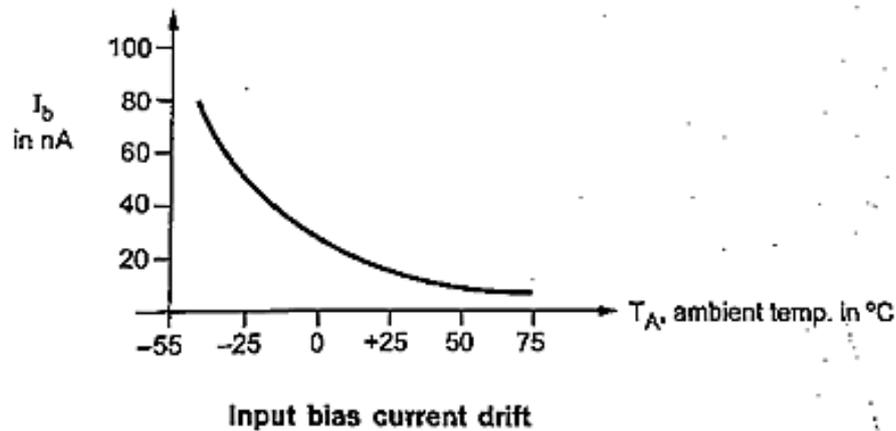
$\rightarrow$ The input offset current is assumed to be zero at room temperature of 25^0C.

$\rightarrow$ Practically no information is available about the change in input bias current versus temperature.

$\rightarrow$ Infact when compensating resistance R_{comp} is used, there is no need to consider the change in input bias current as a function of change in temperature.

3. A.C. CHARACTERISTICS OF OP-AMP:

$\rightarrow$ The important a. c. characteristics of op-amp are,
   i. Slew Rate
   ii. Frequency Response

3.1. Slew Rate:

4. What is slew rate? List the causes of slew rate and explain its significance in applications. (Nov-15)

$\rightarrow$ The slew rate is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/μsec. Thus,

$$Slew\ Rate = S = \frac{dV_0}{dt}\Big|_{max}$$

$\rightarrow$ The slew rate is caused due to limited charging rate of the compensating capacitor and current limiting and saturation of the internal stages of an op-amp, when a high frequency, large amplitude signal is applied.

$\rightarrow$ The internal capacitor voltage cannot change instantaneously. It is given by $\frac{dV_c}{dt} = \frac{1}{C}$. For large charging rate, the capacitor should be small or charging current should be large.

$\rightarrow$ Hence the slew rate for the op-amp whose maximum internal capacitor charging current is known, can be obtained as

$$S = \frac{I_{max}}{C}$$

3.1.1 Effect of Slew Rate:

$\rightarrow$ Consider a circuit using op-amp having **unity gain**. Thus output is same as input. If the input is square wave, output has to be square wave.

$\rightarrow$ But this is observed for certain frequency of input. Due to slew rate of an op-amp, for a particular input frequency, output gets distorted as shown in the Fig.
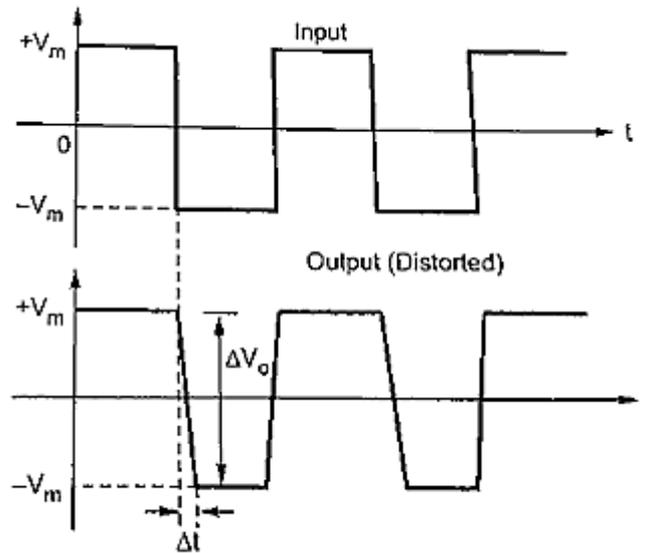
Effect of slew rate

→ Then observing such a distorted waveform on CRO the slew rate can be obtained as,

$$S = \frac{\Delta V_0}{\Delta t} \quad V/\mu sec$$

→ The typical value of S for IC 741 op-amp is 0.5×10^6 V / sec i.e. 0.5 V/µsec. ideally, it should be infinite.

→ **Key Point:** Higher the value of S better is the performance of op-amp.

3.1.2 Slew Rate Equation:

→ Consider unity gain op-amp circuit with purely sinusoidal input. The output must be same as input.

$$V_s = V_m \sin \omega t$$
$$V_o = V_m \sin \omega t$$
$$\therefore \quad \frac{dV_o}{dt} = V_m (\omega co\, s\, \omega t)$$

But

$$Slew\ Rate = S = \left.\frac{dV_0}{dt}\right|_{max}$$

The third equation has maximum value when cosωt = 1.

$$\therefore \quad S = V_m \omega = 2\pi f V_m$$
$$\therefore \quad S = 2\pi f V_m \quad V/\mu sec$$

This is the slew rate equation.

→ For distortion free output, the maximum allowable input frequency f_m can be obtained as,

$$\therefore \quad f_m = \frac{S}{2\pi V_m} \quad Hz$$

→ This is also called **full power bandwidth** of the op-amp. The V_m is peak of output waveform.

3.2. Frequency Response of Op-amp:

→ Ideally, an op-amp should have an infinite bandwidth. This means the gain of op-amp must remain same for all the frequencies from zero to infinite.

→ Till now we have assumed gain of the op-amp as constant but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called **roll off**.

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→ This happens because gain of the op-amp depends on the frequency and hence mathematically it is a complex number.

→ Its magnitude and the phase angle changes with the frequency.

→ The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called **frequency response** of the op-amp.

→ In such plots, to accommodate large range of frequency, it is plotted on a logarithmic scale.

→ The gain magnitude can be plotted as a numerical value or may be expressed in decibels. When the gain in decibels, phase angle in degrees is plotted against logarithmic scale of frequency, the plot is called **Bode plot**.

→ The manner in which the gain of the op-amp changes with variation in frequency is known as the **magnitude plot** and the manner in which the phase shift changes with variation in frequency is known as the **phase angle plot**.

→ Generally magnitude plot is supplied by the manufacturers. The dependence of gain of the op-amp on frequency is basically because of presence of capacitive component in the equivalent circuit of the op-amp.

→ As Op-amp uses BJT and FET, which have the junction capacitances which is very small, but at high frequency, these offer decreased reactance.

→ Not only the BJT and FET, but the construction of op-amp also contributes to the presence of capacitance.

→ All the resistors and transistors in op-amp are fabricated on the material called substrate which acts as an insulator.

→ Similarly there are conducting material wires, connecting the various components. The two conductors separated by an insulator produce capacitive effect.

→ Hence overall there exists a capacitive effect in the op-amp. To obtain the frequency response, consider the high frequency model of the op-amp with a capacitor C at the output, taking into account the capacitive effect present. It is shown in the Fig.
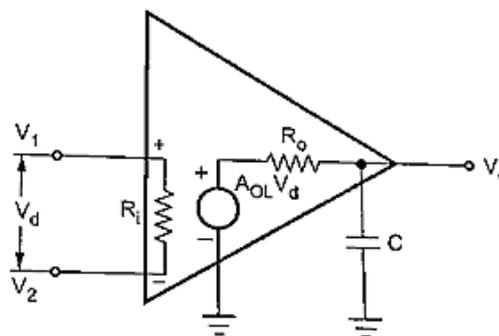
High frequency model of op-amp

→ Let $-jX_C$ be the capacitive reactance due to the capacitor C. From the above Fig. using voltage divider rule,

$$V_o = -jX_C \left[\frac{A_{OL}V_d}{R_O - jX_C} \right]$$

Now, $\qquad -j = \frac{1}{j} \qquad$ and $\qquad X_C = \frac{1}{2\pi f C}$

$$V_o = \frac{\frac{1}{j2\pi fC}}{R_O + \frac{1}{j2\pi fC}} (A_{OL}V_d)$$

$$\therefore \quad V_o = \frac{A_{OL}V_d}{1 + j2\pi fCR_O}$$

→ Hence the open loop voltage gain as a function of frequency is,

$$A_{OL}(f) = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi fCR_O}$$

Let, $\quad f_0 = \frac{1}{2\pi R_O C}$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j\left(\frac{f}{f_0}\right)}$$

Where, $A_{OL}(f)$ = Open loop gain as a function of frequency

$\quad A_{OL}$ = Gain of op-amp at 0 Hz i.e. d.c.

$\quad$ f = Operating frequency

$\quad f_0$ = Break frequency or cut off frequency of op-amp

→ For a given op-amp and selected value of C, the frequency f_0 is constant. The above equation can be written in polar form as,

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_0}\right)^2}}$$

$$< A_{OL}(f) = \emptyset(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$$

At f = 0 Hz, the magnitude is $A_{OL,}$ while $\emptyset(f) = 0^0$.

→ For IC 741 op-amp, f_0 = 5 Hz and the open loop gain 200,000, we can calculate gain and phase shifts at various frequencies as given below:

Frequency, f (Hz)	$|A_{OL}(f)| = 20\log\frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_0}\right)^2}}$ (dB)	$\emptyset(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$ (degrees)
0	106.02 dB	0^0
5	103.01dB	-45^0
10	99.03dB	-63.43^0
100	79.98dB	-87.13^0
1000	60.00dB	-89.71^0
100×10^3	20.00dB	-89.99^0
1×10^6	0dB	-89.999^0

→ As the frequency increases till f_0, the gain is almost constant but after f_0, the gain reduces with a rate of -20 dB/ decade.

→ The maximum possible phase shift is -90°.Hence the frequency response is shown as in the Fig.

Frequency response of an op-amp
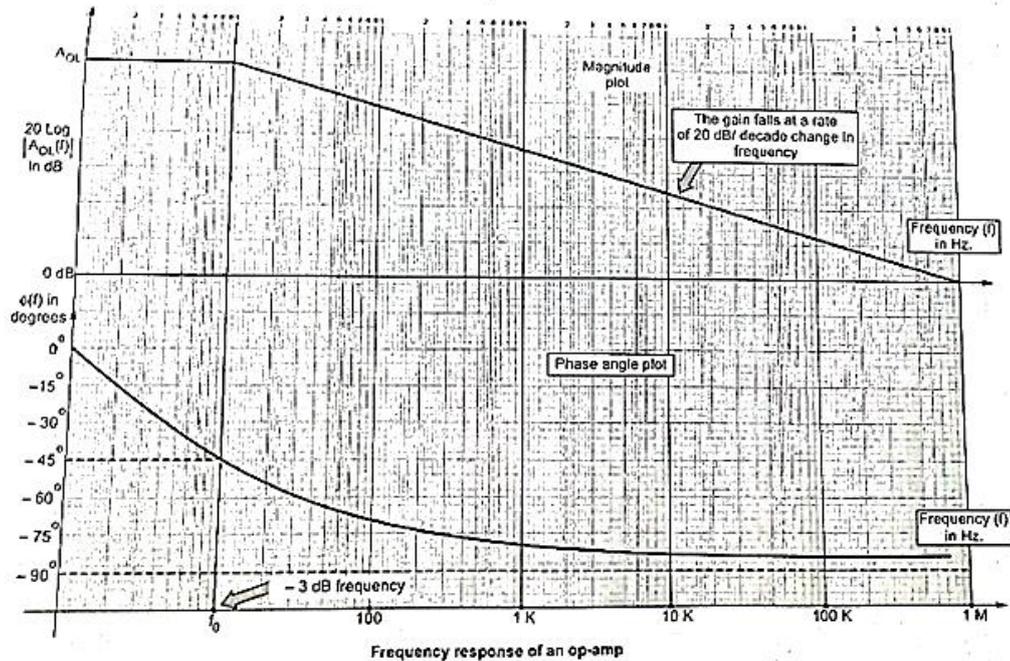
→ The following observations can be made from the frequency response of an op-amp:

i) The open loop gain A_{OL} is almost constant from 0 Hz to the break frequency f_0.

ii) At $f = f_0$, the gain is 3 dB down from its value at 0 Hz. Hence the frequency f_0 is also called as **-3 dB frequency**. It is also known as **corner frequency**.

iii) After $f = f_0$, the gain A_{OL} (f) decreases at a rate of 20 dB / decade or 6 dB / octave. A decade is 10 times change in frequency while octave is 2 times change in frequency. As gain decreases, slope of the magnitude plot is -20 dB/ decade or -6 dB/ octave, after $f = f_0$.

iv) At a certain frequency, the gain reduces to 0 dB. This means 20 log $|A_{OL}$ (f)| is 0 dB i.e. $|A_{OL}$ (f)| = 1. Such a frequency is called **gain cross-over frequency** or **unity gain bandwidth (UGB)**. It is also called **closed loop bandwidth**. UGB is the **gain bandwidth product** only if an op-amp has a single break frequency, before A_{OL} (f) dB is zero.

→ For an op-amp with single break frequency f_0, after f_0 the gain bandwidth product is equal to UGB.

$$UGB = A_{OL} f_0$$

→ The op-amp for which there is only one change in the slope of the magnitude plot is called as **single break frequency op-amp**.

→ For a single break frequency, we can write,

$$UGB = A_f f_f$$

Where, A_f = Closed loop voltage gain

f_f = Bandwidth with feedback

v) The phase angle of an op-amp with a single break frequency varies between 0^0 and 90^0. The maximum possible phase shift is -90^0, i.e. output voltage lags input voltage by 90^0 when phase shift is maximum.

vi) At a corner frequency $f = f_0$, the phase shift is -45^0.

> 5. **Draw the circuit of differential amplifier and derive the expression for output voltage in it. (8)**

4. DIFFERENTIAL AMPLIFIER:

$\rightarrow$ The differential amplifier amplifies the difference between two input voltage signals. Hence it is also called difference amplifier. Consider an ideal differential amplifier shown in the Fig.

A differential amplifier
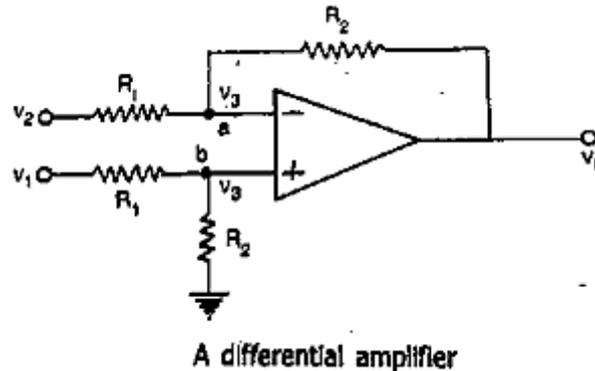
$\rightarrow$ V_1 and V_2 are the two input signals while V_0 is the single ended output. Each signal is measured with respect to the ground.

$\rightarrow$ In an ideal differential amplifier, the output voltage V_0 is proportional to the difference between the two input signals. Hence we can write,

$$V_0 \propto (V_1 - V_2)$$

4.1 Features of Differential Amplifier:

The various features of a differential amplifier are:

1. High differential voltage gain
2. Low common mode gain
3. High CMRR
4. Two input terminals
5. High input impedance
6. Large bandwidth
7. Low offset voltages and currents
8. Low output impedance

4.2 Transistorised Differential Amplifier:

$\rightarrow$ The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics.

$\rightarrow$ Such two identical emitter biased circuits are shown in the Fig.The two transistors Q_1 and Q_2 have exactly matched characteristics.

$\rightarrow$ The two collector resistances R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal. Thus, $R_{C1} = R_{C2}$ and $R_{E1} = R_{E2}$

$\rightarrow$ The magnitudes of $+ V_{CC}$ and $- V_{EE}$ are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting emitter E_1 of Q_1 to the emitter E_2 of Q_2.

$\rightarrow$ Due to this, R_{E1} appears in parallel with R_{E2} and the combination can be replaced by a single resistance denoted as R_E.

$\rightarrow$ The base B_1 of Q_1 is connected to the input 1 which is V_{S1} while the base B_2 of Q_2 is connected to the input 2 which is V_{S2}.
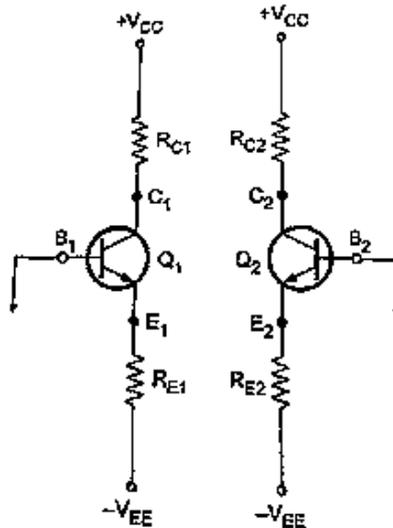
Emitter biased circuits

→ The supply voltages are measured with respect to ground. The balanced output is taken between the collector C_1 of Q_1 and the collector C_2 of Q_2.

→ Such an amplifier is called emitter coupled differential amplifier. The two collector resistances are same hence can be denoted as R_C.

→ The output can be taken between two collectors or in between one of the two collectors and the ground.

→ When the output is taken between the two collectors, none of them is grounded then it is called **balanced output, double ended output or floating output.**

→ When the output is taken between any of the collectors and the ground, it is called **unbalanced output or single ended output**.

→ The complete circuit diagram of such a basic dual input, balanced output differential amplifier is shown in the Fig.
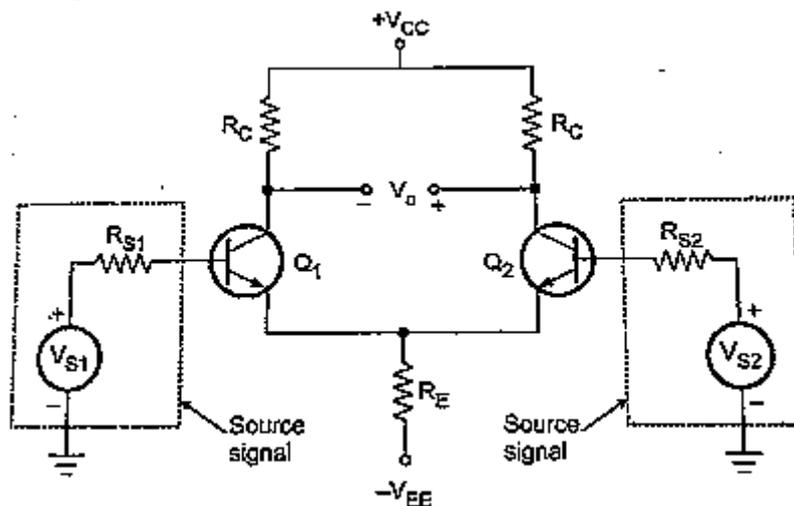
Dual input, balanced output differential amplifier

→ As the output is taken between two output terminals, none of them is grounded, it is called **balanced output differential amplifier**.

→ Let us study the circuit operation in the two modes namely:
   ❖ Differential mode operation
   ❖ Common mode operation.

4.3 Modes of operation:
4.3.1 Differential Mode Operation:
   $\rightarrow$ In the differential mode, the two input signals are different from each other.
   $\rightarrow$ Consider the two input signals which are same in magnitude but 180° out of phase.
   $\rightarrow$ These signals, with opposite phase can be obtained from the center tap transformer.
   $\rightarrow$ The circuit used in differential mode operation is shown in the Fig.
   $\rightarrow$ Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 it is negative going.
   $\rightarrow$ With a positive going signal on the base of Q_1, an amplified negative going signal develops on the collector of Q_1.
   $\rightarrow$ Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E.
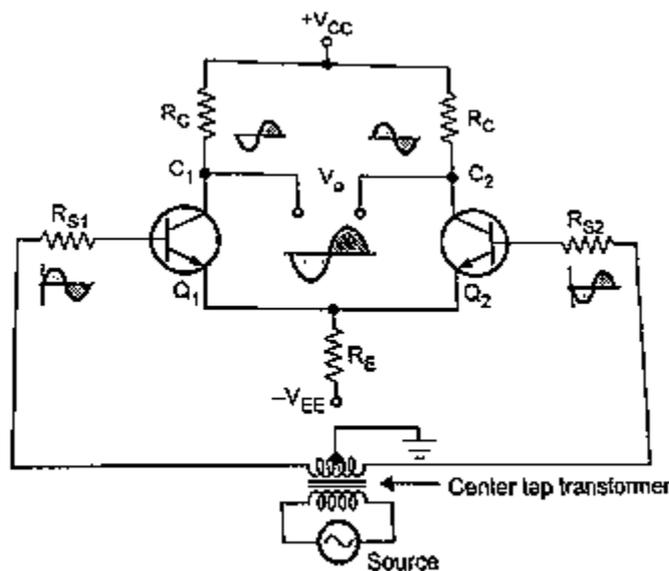
Differential mode operation

   $\rightarrow$ Due to negative going signal on the base of Q_2, an amplified positive going signal develops on the collector of Q_2.
   $\rightarrow$ And a negative going signal develops across R_E, because 0f emitter follower action of Q_2.
   $\rightarrow$ So signal voltages across R_E, due to the effect of Q_1 and Q_2 are equal in magnitude and 180° out of phase, due to matched pair of transistors.
   $\rightarrow$ Hence these two signals cancel each other and there is no signal across the emitter resistance.
   $\rightarrow$ Hence there is no a.c. signal current flowing through the emitter resistance. Hence R_E in this case does not introduce negative feedback.
   $\rightarrow$ While V_0 is the output taken across collector of Q_1 and collector of Q_2, the two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity.
   $\rightarrow$ And V_0 is the difference between these two signals, e.g. +10 - (-10) = + 20.

Key Point: Hence the difference output V_0 is twice as large as the signal voltage from either collector to ground.

4.3.2 Common Mode Operation:
   $\rightarrow$ In this mode, the signals applied to the base of Q_1 and Q_2 are derived from the same source.

→ So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

→ In-phase signal voltages at the bases of Q_1 and Q_2 causes an in-phase signal voltage to appear across R_E, which are added together.

→ Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

Common mode operation
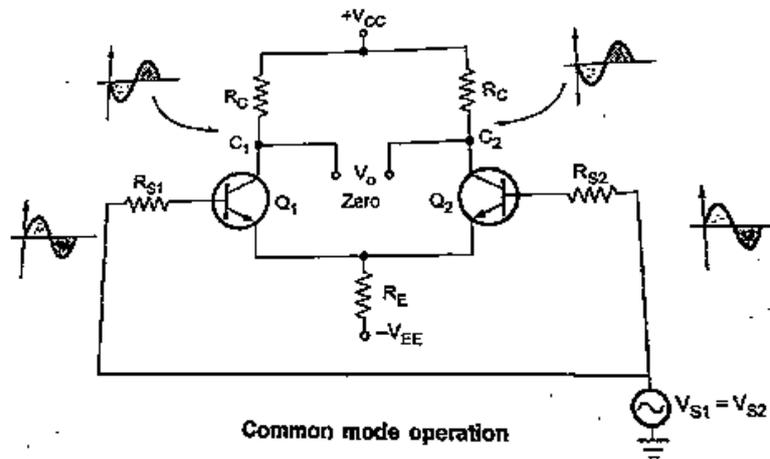
→ While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q_2, the output voltage is the difference between the two collector voltages, which are equal and also same in phase, e.g. $(10) - (10) = 0$.

→ Thus the difference output V_0 is almost zero, negligibly small. **Ideally it should be zero**.

4.4 D.C. ANALYSIS OF DIFFERENTIAL AMPLIFIER:

6. Draw the circuit of a symmetrical emitter coupled differential amplifier and derive for CMRR. (Nov-17) (16)

(or)

Explain the working principles of emitter coupled differential amplifier. (May-18) (7)

→ The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used.

→ The supply voltages are d.c. while the input signals are a.c., so d.c. equivalent circuit can be obtained simply by reducing the input a.c. signals to zero.

→ The d.c. equivalent circuit thus obtained is shown in the figure below.

→ Assuming $R_{S1} = R_{S2}$, the source resistance is simply denoted by R_S.

→ The transistors Q_1 and Q_2 are matched transistors and hence for such a matched pair we can assume:

  ❖ Both the transistors have the same characteristics.

  ❖ $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \parallel R_{E2}$.

  ❖ $R_{C1} = R_{C2}$ hence denoted as R_C.

  ❖ $\left| V_{CC} \right| = \left| V_{EE} \right|$ and both are measured with respect to ground.

D.C. equivalent circuit

→ As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors.

→ The same is applicable for the other transistor.

→ Applying KVL to base-emitter loop of the transistor Q_1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad (1)$$

But, $I_C = \beta I_B$ and $I_C \approx I_E$

$$\therefore \ I_B = \frac{I_E}{\beta} \quad (2)$$

Substituting I equation (1), we get,

$$\frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad (3)$$

$$\therefore \ I_E \left[\frac{-R_S}{\beta} - 2R_E \right] + V_{EE} - V_{BE} = 0 \quad (4)$$

$$\therefore \ I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \quad (5)$$

where, $V_{BE} = 0.6$ to 0.7 V for silicon

                    $= 0.2$ V for germanium

→ In practice, generally $R_S / \beta \ll 2R_E$

$$\therefore \ I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad (6)$$

→ From the equation (6), we can observe that,

❖ R_E determines the emitter current of Q_1 and Q_2 for the known value of V_{EE}.

❖ The emitter current through Q_1 and Q_2 is independent of collector resistance R_C.

→ Now let us determine V_{CE}. As I_E is known and $I_E \approx I_C$, we can determine the collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad (7)$$

→ Neglecting the drop across R_S, we can say that the voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$. Hence the collector to emitter voltage is

$$V_{CE} = V_C - V_E = V_{CC} - I_C R_C - (-V_{BE})$$

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$$V_{CE} = V_{CC} - I_C R_C + V_{BE} \qquad (8)$$

→ Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.

→ In the equation (6), the sign of V_{EE} is already considered to be negative, while deriving it.

→ Hence while using this equation to solve the problem, only the magnitude of V_{EE} should be used and negative sign of V_{EE} should not be used again.

→ Thus for both the transistors, we can determine operating point values, using equations (6) and (8).

4.5 A.C. ANALYSIS USING h-PARAMETERS:

→ In the A.C. analysis, we will calculate the differential gain A_d, common mode gain A_c, of the differential amplifier circuit, using the h-parameters.

4.5.1 Differential mode Gain (A_d):

→ The a.c. equivalent circuit of a differential amplifier is given as follows:
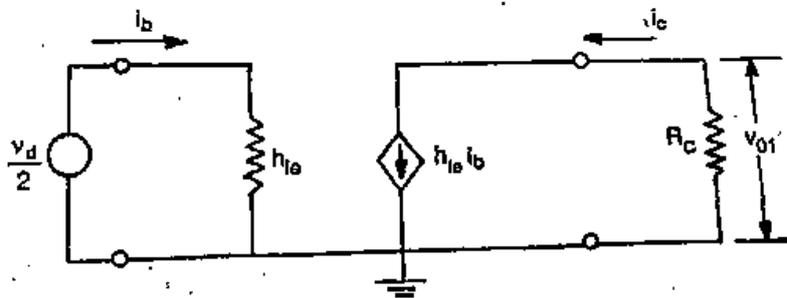
Small signal equivalent circuit of differential half circuit using
h-parameter model

From the figure, $\qquad v_{01} = -i_C R_C = -h_{fe} i_b R_C$

And $\qquad \dfrac{v_d}{2} = i_b h_{ie}$

Therefore, the differential mode gain, A_{DM} is given by

$$A_d = \frac{v_{01}}{v_d} = -\frac{1}{2}\frac{h_{fe}}{h_{ie}} R_C \quad (Single\ ended\ output)$$

Similarly, we may write,

$$A_d = \frac{v_{02}}{v_d} = \frac{1}{2}\frac{h_{fe}}{h_{ie}} R_C \quad (Single\ ended\ output)$$

The output is taken differentially between the two collectors, then

$$A_d = \frac{v_{01} - v_{02}}{v_d} = -\frac{h_{fe}}{h_{ie}} R_C \quad (differential\ output)$$

In the above analysis, the source resistance R_S has not been taken into account.

4.5.2 Common mode Gain (A_c):

→ Now consider the case when v_1 and v_2 both are increased by an incremental voltage v_c.

→ The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_C.

→ The current through R_E now increases by $2i_C$.
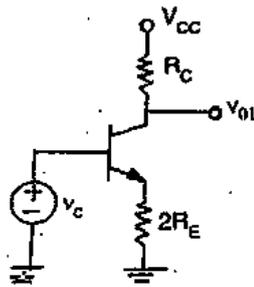
common-mode half circuit

→ The voltage, V_E at emitter node is now $2i_C R_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in figure above.

→ The common mode gain, A_c, using h-parameter model can be easily computed as,

$$A_c = \frac{v_{01}}{v_c} = \frac{-h_{fe}R_C}{h_{ie} + 2(1 + h_{fe})R_E}$$

→ It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common mode gain will be zero.

→ However, if the output is taken single ended, the common mode gain will be finite.

4.5.3 CMRR:

7. How the CMRR increased using constant current source? (May-18) (6)

→ CMRR means Common Mode Rejection Ratio.

→ The ability of the differential amplifier to reject common mode signals is expressed by the ratio of differential gain to common mode gain which is called its Common Mode Rejection Ratio (CMRR).

→ It is defined as the ratio of differential voltage gain A_d to common mode voltage gain A_c.

$$CMRR = \rho = \left| \frac{A_d}{A_c} \right|$$

→ Ideally the common mode voltage gain is zero and hence the ideal value of CMRR is infinite.

→ For a differential input, differential output, we get,

$$CMRR \cong \frac{-\frac{h_{fe}}{h_{ie}}R_C}{\frac{-h_{fe}R_C}{h_{ie}+2(1+h_{fe})R_E}}$$

$$CMRR = \frac{h_{ie} + 2(1 + h_{fe})R_E}{h_{ie}}$$

$$CMRR = 1 + \frac{2(1 + h_{fe})R_E}{h_{ie}}$$

$$CMRR \cong \frac{2(1 + h_{fe})R_E}{h_{ie}}$$

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5. FREQUENCY COMPENSATION:

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8. Explain the frequency compensation techniques of OP-AMP. (Dec – 12) (16)

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(or)

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Explain in detail about various methods of frequency compensation used in operational amplifiers. (May-15, 17) (Dec-15) (8)

→ In order to obtain larger bandwidth and low voltage gain, compensation is required. There are mainly two compensations required namely:

❖ External Compensation

❖ Internal Compensation

5.1 External Compensation Technique:

→ As mentioned earlier, the compensating network is connected to the system externally to alter the response as per the requirement.

→ There are three such external compensation techniques used in practice.

1) Dominant pole compensation

2) Pole-Zero compensation

3) Feed-forward compensation

5.1.1 Dominant Pole Compensation:

→ Consider an op-amp with three break frequencies and its loop gain is say A.

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

→ In this loop gain, the dominant pole is introduced by adding a compensating network. Such a network is nothing but a simple R-C network as shown in the Fig.

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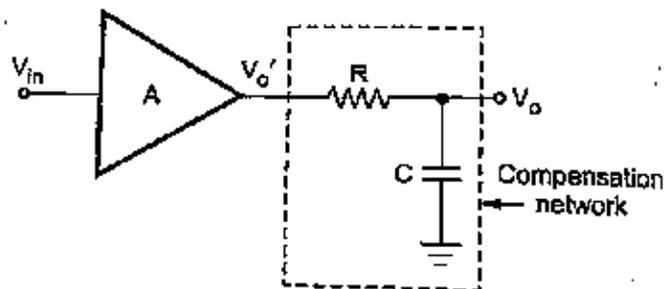
Dominant pole compensation

</div>

→ The dominant pole means the pole with magnitude much smaller than the existing poles.

→ Hence the break frequency of the compensating network is the smallest compared to the existing break frequencies.

→ The transfer function of the compensating network can be obtained as:

A_1 = Transfer function of compensating network

$$A_1 = \frac{V_o}{V_o'}$$

By the voltage divider rule applied to the network,

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_C}{R - jX_C}$$

<div align="center">

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$$= \frac{-\frac{j}{2\pi f C}}{R - \frac{j}{2\pi f C}} = \frac{1}{\frac{R}{\left(-\frac{j}{2\pi f C}\right)} + 1}$$

As $\quad \frac{1}{-j} = j$, we can write

$$\therefore \quad A_1 = \frac{1}{1 + j\left(\frac{f}{f_d}\right)}$$

Where, f_d = break frequency of the compensating network

$\rightarrow$ Hence the compensated transfer function becomes,

$$A' = AA_1$$

$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

Where, $\qquad f_d < f_1 < f_2 < f_3.$

$\rightarrow$ The compensated and uncompensated magnitude plots are shown in Fig.
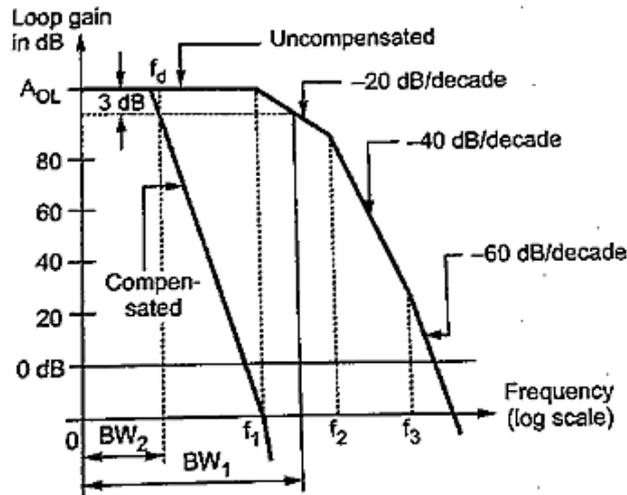
Dominant pole compensation

$\rightarrow$ It can be observed from the plot that 3 dB down bandwidth for non-compensated system is BW_1 while for compensated it becomes BW_2. There is drastic reduction in the bandwidth.

Advantages:
- ❖ As the noise frequency components are outside the smaller bandwidth, the noise immunity of the system improves.
- ❖ Adjusting value of f_d, adequate phase margin and the stability of the system is assured.

Disadvantage:
- ❖ The only disadvantage of the method is that the bandwidth reduces drastically, as mentioned earlier.

5.1.2 Pole Zero Compensation:

$\rightarrow$ Consider the same op-amp described by the open loop gain A with three break frequencies as

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

$\rightarrow$ In this method, the transfer function A is modified by adding a pole and a zero with the help of compensating network.

→ The zero added is at higher frequency while a pole is at lower frequency. Such a compensating network is shown in the Fig.
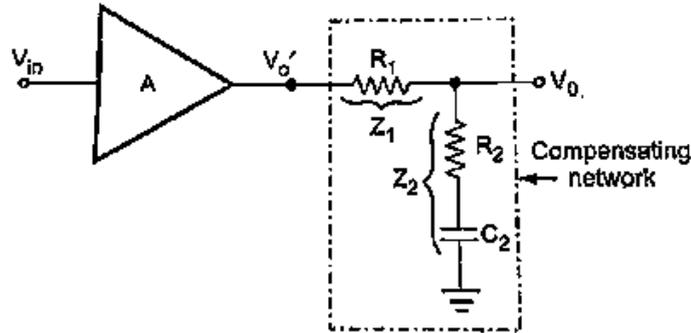
Pole-Zero compensation

Let the transfer function of the compensating network be A_1:

$$A_1 = \frac{V_o}{V_o'}$$

By the voltage divider rule,

$$A_1 = \frac{Z_2}{Z_1 + Z_2}$$

Now, $Z_2 = R_2 - jX_{C2}$ and $Z_1 = R_1$

$$\therefore \quad A_1 = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}} = \frac{R_2 - \frac{j}{2\pi f C_2}}{R_1 + R_2 - \frac{j}{2\pi f C_2}} = \frac{\frac{R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}{\frac{R_1 + R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}$$

Now, $\frac{1}{-j} = j$

$$\therefore \quad A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) C_2}$$

Now let $f_1 = \frac{1}{j2\pi R_2 C_2}$ and $f_0 = \frac{1}{j2\pi (R_1 + R_2) C_2}$

$$\therefore \quad A_1 = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_0}\right)}$$

→ The values of R_1, R_2 and C_2 are so selected that the break frequency for the zero matches with the first corner frequency f_1 of the uncompensated system.

→ While the pole of the compensating network at f_o is selected in such a way that the compensated transfer function **A'** passes through 0 dB at the second corner frequency f_2 of the uncompensated system.

→ The resultant loop gain becomes,

$$A' = AA_1$$

$$A_1 = \frac{A_{OL}\left(1 + j\frac{f}{f_1}\right)}{\left(1 + j\frac{f}{f_0}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

Where, $0 < f_0 < f_1 < f_2 < f_3$.

→ As compared to the dominant pole compensation there is improvement in the bandwidth, equal to $f_2 - f_1$. This is the additional advantage of pole-zero compensation technique.

Pole-zero compensation
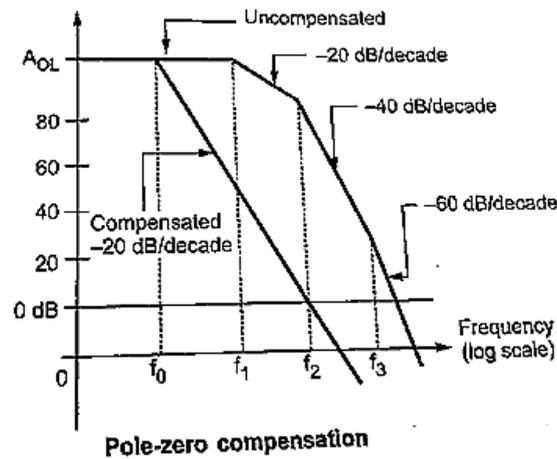
→ The value of compensation capacitor is generally very large.

→ Hence it is not possible to build such capacitor into standard integrated circuits.

→ Generally the connections are brought out from IC to connect the compensation elements externally.

5.2 Internal Compensation Technique:

→ Recently in op-amps like IC 741, the compensation is provided internally, which is generally built in lag compensation.

→ A capacitor ranging from 10 to 30 pF is fabricated between input and output stage to achieve the necessary compensation.

→ This type of compensation is called **Miller effect compensation**. Such op-amps are called **compensated op-amps**.

5.2.1 Miller Effect Compensation:

→ The main drawback of dominant pole compensation is the reduction in the bandwidth.

→ Similarly the value of capacitance required in this method is very large and fabricating such large capacitance on the chip is not practicable.

→ These drawbacks are avoided by using Miller effect compensation, using the Miller effect.

→ In dominant pole compensation, a capacitor is connected to ground from the output terminal but in Miller effect compensation it is connected in the feedback path of the Darlington pair used in the output stage of op-amp.

→ This is shown in the Fig.

Miller Effect Compensation
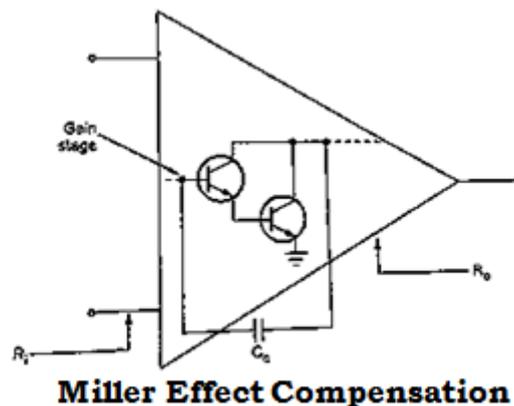
→ The C_C is the compensating capacitor, R_i is the input resistance and R_0 is the output resistance of the Darlington stage. The gain of the Darlington stage is given by,

$$a_2 = -G_{mc}R_0$$

Where G_{mc} = Trans-conductance of the stage

→ Looking through the input terminal C_C appears as the Miller capacitance C_M and from the results of Miller effect we can write,

$$Z_{C_M} = \frac{Z_{C_C}}{1 + a_2}$$

Where $\qquad Z_{C_M} = \frac{1}{j\omega C_M}$ and $Z_{C_C} = \frac{1}{j\omega C_C}$

$$\therefore \quad \frac{1}{j\omega C_M} = \frac{\frac{1}{j\omega C_C}}{1 + a_2}$$

$$\therefore C_M = (1 + a_2)C_C$$

→ Thus effectively C_C gets multiplied by $(1 + a_2)$ where a_2 is the gain of the stage which is large, as viewed through the input terminals.

→ Thus practically small C_C values can be used, which is helpful from monolithic fabrication point of view.

→ This Miller equivalent capacitance C_M forms a low pass RC section with input resistance R_i whose corner frequency is given by,

$$f_d = \frac{1}{2\pi C_M R_i}$$

→ The uncompensated and compensated magnitude plots are shown in the Fig.
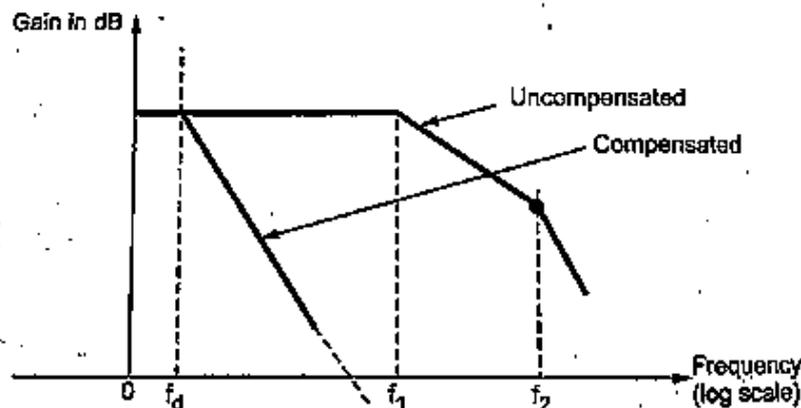
Miller effect compensation

→ In addition to the multiplying the capacitance, Miller effect has another advantage. It causes rearrangement of original poles and cause **Pole splitting**.

→ This means due to Miller effect compensation, f_1 gets lowered while f_2 gets raised. Thus poles get diverged.

→ This increases the bandwidth compared to dominant pole compensation.

→ Such compensated op-amps usually have single break frequency and are inherently stable in nature irrespective of value of closed loop gain.

→ External compensating network is not required for such op-amps.

→ Some internally compensated op-amps are Fairchild's μA 741, National semiconductor's LM 107, LM 741, LM 112 and Motorola's MC 1858.

6. BASIC APPLICATIONS OF OP-AMP
6.1 INVERTING AND NON- INVERTING AMPLIFIERS

9. Explain the Significance of virtual ground in basic inverting OPAMP. How would you explain its existence?

(or)

Draw the inverting amplifier circuit of an op- amp in closed loop configuration. Obtain the expression for closed loop gain. (May-18) (7)

(or)

Explain with neat circuit expression about the working of inverting Amplifier. [Apr/May 2019]

(or)

Illustrate with neat diagram, the working of inverting and Non- inverting amplifiers by using OP- AMPs. Develop the expressions for output voltages. (Nov/Dec 2019)

6.1.1 INVERTING AMPLIFIER:

→ This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig.
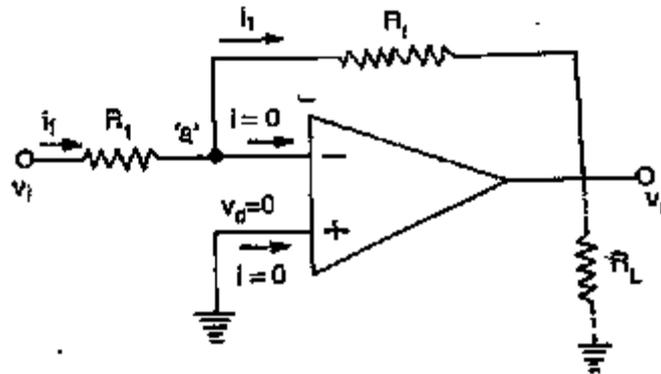
Inverting amplifier

→ The output voltage v_0 is fed back to the inverting input terminal through the R_f– R_1 network where R_f is the feedback resistor.

→ Input signal v_i is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

→ **Analysis:** For simplicity, assume an ideal op-amp. As $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1} \rightarrow (1)$$

→ Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage,

$$v_0 = -i_1 R_f = -v_i \frac{R_f}{R_1} \rightarrow (2)$$

→ Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_0}{v_i} = -\frac{R_f}{R_1} \rightarrow (3)$$

→ Alternatively, the nodal equation at the node 'a' in Fig. is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_0}{R_f} = 0$$

Where v_a is the voltage at node 'a'.

→ Since node 'a' is at virtual ground $v_a = 0$. Therefore, we get,

$$A_{CL} = \frac{v_0}{v_i} = -\frac{R_f}{R_1}$$

→ The negative sign indicates a phase shift of 180^0 between v_i and v_0. Also since inverting terminal is at virtual ground, the effective input impedance is R_1.

→ The value of R_1 should be kept fairly large to avoid loading effect.

→ This however, limits the gain that can be obtained from this circuit.

→ A load resistor R_L is usually put at the output in actual practice otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load.

→ If, however, resistances R_1 and R_f in Fig. are replaced by impedances Z_1 and Z_f respectively, then the voltage gain, A_{CL} will be

$$A_{CL} = \frac{Z_f}{Z_i} \rightarrow (4)$$

→ This expression for the voltage gain will be used in op-amp application, such as integrator, differentiator etc.

6.1.1.1 Practical Inverting Amplifier:

→ The gain of the inverting amplifier given above is valid only if the op-amp is an ideal one.

→ For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of the followingFig.
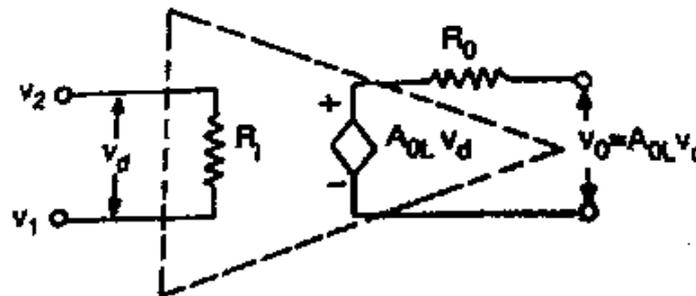
Equivalent circuit of an op-amp

→ The equivalent circuit of a practical inverting amplifier is shown in Fig. below,
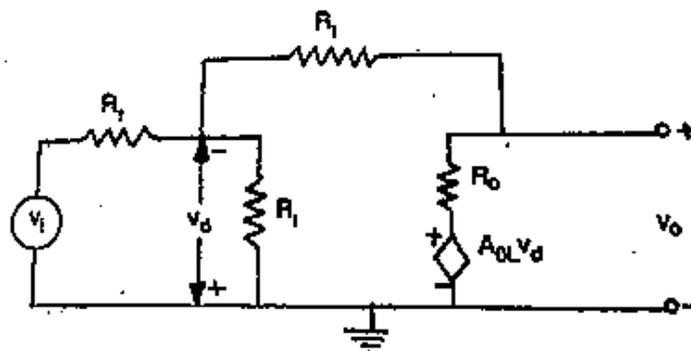
Equivalent circuit of a practical op-amp inverting amplifier

→ This circuit can be simplified by replacing the signal source v_i and resistors R_1 and R_i by Thevenin's equivalent as shown in Fig. below, which is analysed to calculate the exact expression for closed loop gain, A_{OL} and input impedance R_{if}.
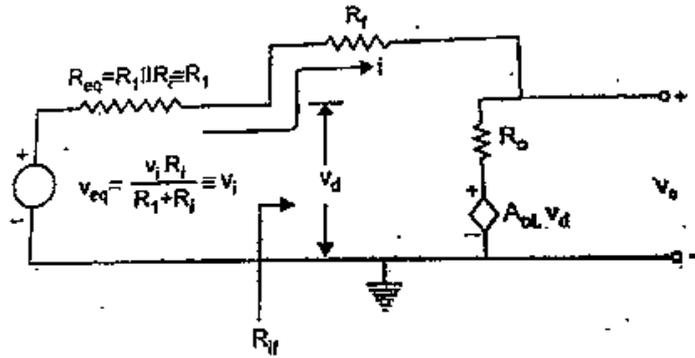
Simplified circuit using Thevenin's equivalent

→ The input impedance R_i of an op-amp is usually much greater than R_1, so one may assume, $v_{eq} \approx v_i$ and $R_{eq} \approx R_1$.

From the output loop in Fig

$$v_0 = iR_0 + A_{OL}v_d \rightarrow (5)$$

Also

$$v_d + iR_f + v_0 = 0 \quad \rightarrow (6)$$

→ Putting the value of v_d from equation (5) to equation (6) and simplifying,

$$v_0(1 + A_{OL}) = i(R_0 - A_{OL}R_f) \quad \rightarrow (7)$$

→ Also the KVL loop equation gives,

$$v_i = i(R_1 + R_f) + v_0 \rightarrow (8)$$

→ Putting the value of **I** from equation (7) in equation (8) and solving for closed loop gain $A_{CL} = \frac{v_0}{v_i}$, gives

$$A_{CL} = \frac{v_0}{v_i} = \frac{R_0 - A_{OL}R_f}{R_0 + R_f + R_1(1 + A_{OL})} \rightarrow (9)$$

→ It can be seen from equation (9) that if $A_{OL} \gg 1$ and $A_{OL} R_1 \gg R_0 + R_f$

$$A_{CL} \approx \frac{R_f}{R_1}$$

6.1.2 NON- INVERTING AMPLIFIER:

→ If the signal is applied to the non-inverting input terminal and feedback is given as shown in Fig., the circuit amplifies without inverting the input signal.

→ Such a circuit is called non-inverting amplifier.

→ It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

Non-Inverting amplifier

40
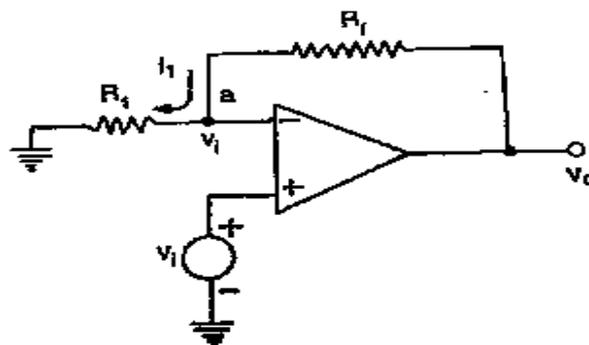
→ As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. is v_i, same as the input voltage applied to non-inverting input terminal.

→ Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_0}{R_1 + R_f} \cdot R_1 \rightarrow (1)$$

→ As no current flows into the op-amp,

$$\frac{v_0}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \rightarrow (2)$$

→ Thus, for a non- inverting amplifier, the voltage gain is,

$$A_{CL} = \frac{v_0}{v_i} = 1 + \frac{R_f}{R_1} \rightarrow (3)$$

→ The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1.

→ Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large ($= \infty$) as the op-amp draws negligible current from the signal source.

6.1.2.1 Practical Non-Inverting Amplifier:
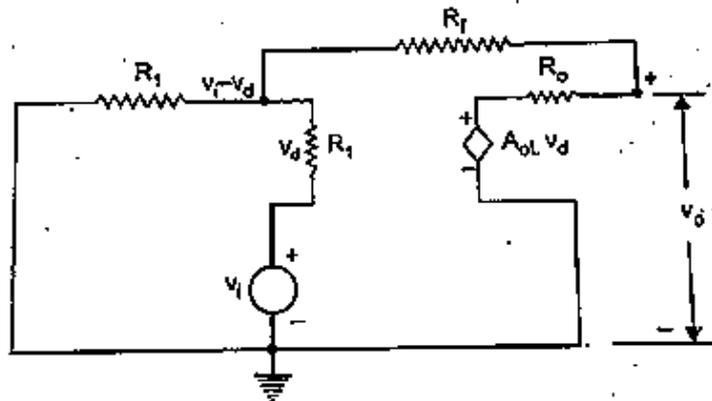
Equivalent circuit of non-inverting amplifier using low frequency model.

→ The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. Writing KCL at the input node,

$$(v_i - v_d)Y_1 + v_d Y_i + (v_i - v_d - v_0)Y_f = 0$$

or

$$-(Y_1 + Y_i + Y_f)v_d + (Y_1 + Y_f)v_i = Y_f v_0 \rightarrow (4)$$

→ Similarly at output node, KCL gives

$$(v_i - v_d - v_0)Y_f + (A_{OL}v_d - v_0)Y_0 = 0$$

$$\therefore \quad -(Y_f - A_{OL}Y_0)v_d + Y_f v_i = (Y_f + Y_0)v_0 \rightarrow (5)$$

→ Now solving equations (4) and (5) for v_0 / v_i, we get

$$A_{CL} = \frac{v_0}{v_i} = \frac{A_{OL}Y_0(Y_1 + Y_f) + Y_i Y_f}{(A_{OL} + 1)Y_0 Y_f + (Y_1 + Y_i)(Y_f + Y_0)} \rightarrow (6)$$

Where, all the admittances have been taken for simplicity.

→ If $A_{OL} \rightarrow \infty$, equation(6) reduces to

$$A_{CL} = \frac{A_{OL}Y_0(Y_1 + Y_f)}{A_{OL}Y_0 Y_f} = \frac{(Y_1 + Y_f)}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$\therefore \quad A_{CL} = 1 + \frac{R_1}{R_f}$$

Which is, the same expression as in equation (3).

PROBLEM:

10. For a given non-inverting amplifier shown in figure below. Determine (i) A_v (ii) V_0 (iii) I_L (iv) I_0 [Apr/May 2019]
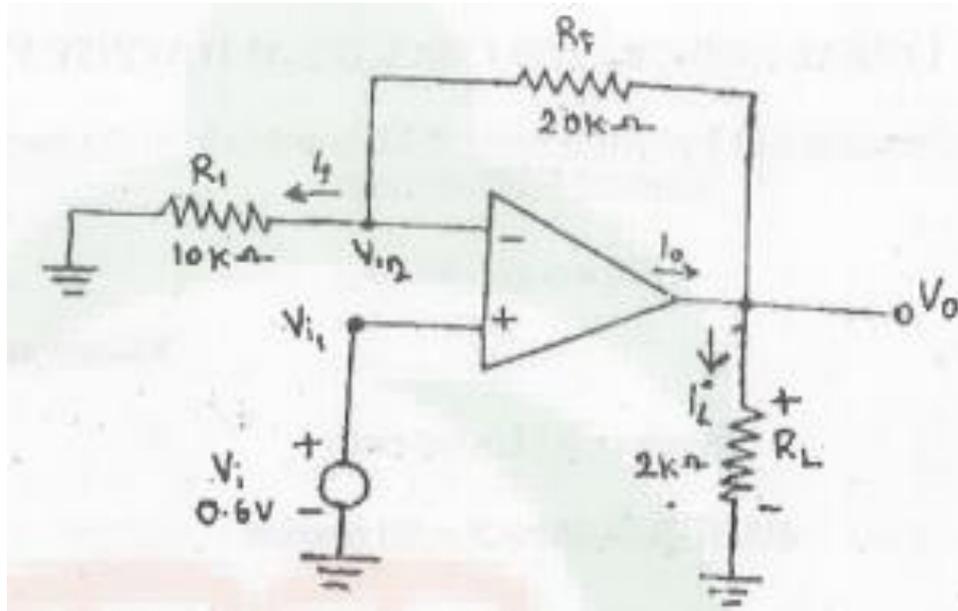
(i) $I_L = V_i / R$
$$= 0.6/10K\Omega$$
$$= 0.6 / 10 * 10^3 \, \Omega$$
$$=0.00006A$$

(ii) $I_0 = V_i / R_L$
$$= 0.6/2K\Omega$$
$$= 0.0003A$$

(iii) $V_0 = (i+Rf/R_1) \cdot V_{in}$
$$= (1+20 \, K\Omega/10 \, K\Omega). \, 0.6V$$
$$=(1+2).0.6V$$
$$= 3(0.6)$$
$$=1.8V$$

(iv) $A_v = V_0 / V_{in}$
$$=1.8V/0.6V$$
$$=3V$$

11. For a non- inverting amplifier shown in fig, R1= 1KΩ, R$_f$= 10 KΩ. Calculate i) the maximum output offset voltage (V$_{os}$= 10mv) and bias current (I$_B$= 300nA) and offset current I$_{os}$ = 50nA. ii) Calcuate the value of R$_{comp}$ need to reduce the effect of I$_B$. iii) Calculate the maximum output offset voltage if R$_{comp}$ is connected in the circuit. Nov/Dec 2019.
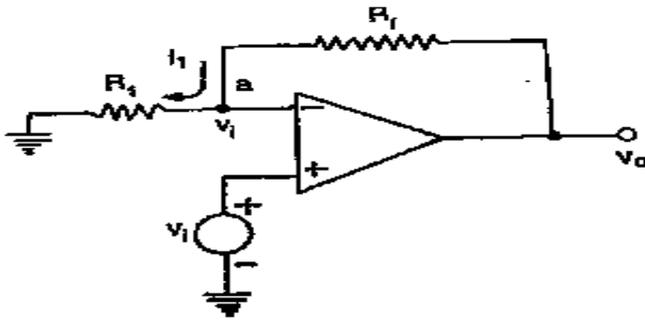
Non-Inverting amplifier

Solution:
Given Data:
R1= 1KΩ
R$_f$= 10 KΩ
Output offset voltage (V$_{os}$= 10mv)
Bias current (I$_B$= 300nA)
Offset current I$_{os}$ = 50nA

   (i)   If R$_{comp}$ is connected,
          Max. Output offset voltage $V_{OT} = (1+(R_f/ R1)) V_{os} + R_f. I_{os}$
                              $V_{OT} = 511 \ \mu V$
   (ii) $R_{comp} = R_1 \| R_f = (R_1 \ x \ R_f) / (R_1 + R_f)$
                   $= (1x \ 10) \ M\Omega / (1+ 10) \ K\Omega$
                   $= 10000000/ 11000$
                   $= 10000/ 11$
                   $= 0.9 \ K\Omega$

   (iii) If R$_{comp}$ is not connected,
          $V_{OT} = (1+(R_f/ R1)) Vios + R_f. I_B$
              $= (1+ 10 \ K\Omega).10mV + (10 \ K\Omega. 300nA)$
              $= 101 + 3000 \ \mu V$
              $= 3101 \ \mu V$

6.2 SUMMERS

12. With the help of circuit diagram show how an OP-AMP is used as a summer. (8)
6.2 SUMMING AMPLIFIER:
   → Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer.
6.2.1 Inverting Summing Amplifier:
   → A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in Fig.
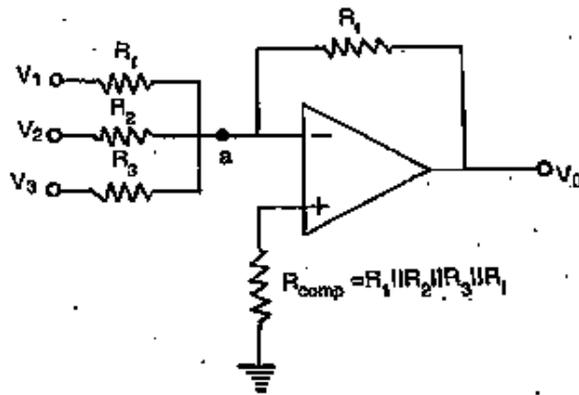
Inverting summing amplifier

→ The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$.

→ Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

→ The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_f} = 0$$

or

$$V_0 = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3$$

→ Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

→ In which case, the output V_0 is the inverted sum of the input signals. We may also set, $R_1 = R_2 = R_3 = 3R_f$, in which case,

$$V_0 = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

→ Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$.

→ So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$. Therefore, $R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$.

6.2.2 Non-Inverting Summing Amplifier:

→ A summer that gives a non-inverted sum is the non-inverting summing amplifier as shown in Fig.

Noninverting summing amplifier

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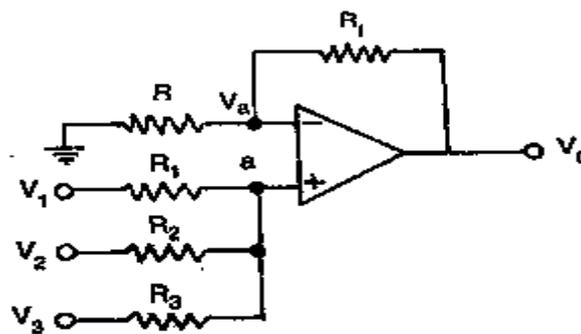
$\rightarrow$ Let the voltage at the (–) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by,

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

$\rightarrow$ The op-amp and two resistors R_f and R constitute a non-inverting amplifier with,

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) \cdot V_a$$

$\rightarrow$ Therefore, the output voltage is,

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) \cdot \left(\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}\right)$$

$\rightarrow$ Which, is a non-inverted weighted sum of inputs.

Let, $R_1 = R_2 = R_3 = R_f/2$, then,

$$V_0 = V_1 + V_2 + V_3.$$

6.3 DIFFERENTIATOR

13. With neat circuit diagram explain the operation of a OP-AMP differentiator and derive and expression for the output of a practical differentiator. (16)

Or

Explain the functions of op-amp as a differentiator. Draw the waveforms. (Dec – 14) (4)

(or)

What are the limitations of ordinary op-amp differentiator? Draw the circuit of practical amplifier which eliminates the limitations. (Nov-15) (8)

6.3 DIFFERENTIATOR:

$\rightarrow$ One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator.

$\rightarrow$ As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform.

$\rightarrow$ A differentiator circuit is shown in Fig.
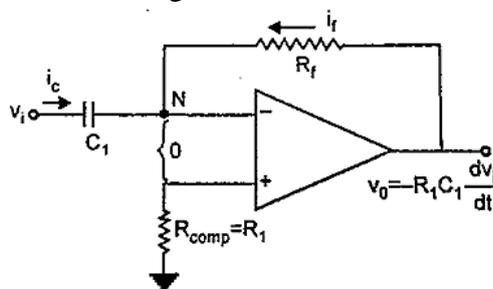
Op-amp differentiator

6.3.1 Analysis:

$\rightarrow$ The node N is at virtual ground potential i.e., $v_n = 0$. The current i_C through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt} \rightarrow (1)$$

→ The current i_f through the feedback resistor is v_0/R_f and there is no current into the op-amp. Therefore, the nodal equation at node N is,

$$C_1 \frac{dv_i}{dt} + \frac{v_0}{R_f} = 0$$

→ From which we have,

$$v_0 = -R_f C_1 \frac{dv_i}{dt} \rightarrow (2)$$

→ Thus the output voltage v_0 is a constant ($-R_f C_1$) times the derivative of the input voltage v_i and the circuit is a differentiator.

→ The minus sign indicates a 180° phase shift of the output waveform v_0, with respect to the input signal.

→ The phasor equivalent of equation (2) is, $V_0(s) = -R_f C_1 s V_i(s)$ where V_0, and V_i is the phasor representation of v_0, and v_i. In steady state, put $s = j\omega$.

→ We may now write the magnitude of gain A of the differentiator as,

$$|A| = \left|\frac{V_0}{V_i}\right| = \left|-j\omega R_f C_1\right| = \omega R_f C_1 \rightarrow (3)$$

→ From equation (3), one can draw the frequency response of the op-amp differentiator. Equation (3) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where,

$$f_a = \frac{1}{2\pi R_f C_1} \rightarrow (4)$$

→ At $f = f_a$, $|A| = 1$, i.e., 0 dB, and the gain increases at a rate of +20 dB/decade.

→ Thus at high frequency, a differentiator may become unstable and break into oscillation.

→ There is one more problem in the differentiator of Fig.

→ The input impedance (i.e., $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

6.3.2 Practical Differentiator:

→ A practical differentiator of the type shown in Fig. eliminates the problem of stability and high frequency noise.

Practical differentiator
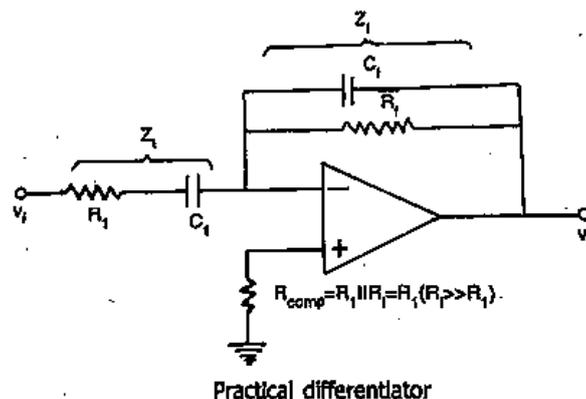
→ The transfer function for the circuit in Fig. is given by,

$$\frac{V_0(s)}{V_i(s)} = -\frac{Z_f}{Z_i} = -\frac{sR_fC_1}{(1 + sR_fC_f)(1 + sR_1C_1)} \to (5)$$

For $R_fC_f = R_1C_1$, we get,

$$\frac{V_0(s)}{V_i(s)} = -\frac{sR_fC_1}{(1 + sR_1C_1)^2} = -\frac{sR_fC_1}{\left(1 + j\frac{f}{f_b}\right)^2} \to (6)$$

where,

$$f_b = \frac{1}{2\pi R_1C_1} \to (7)$$

→ From equation (6)it is evident that the gain increases at +20 dB/decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig.

Frequency response
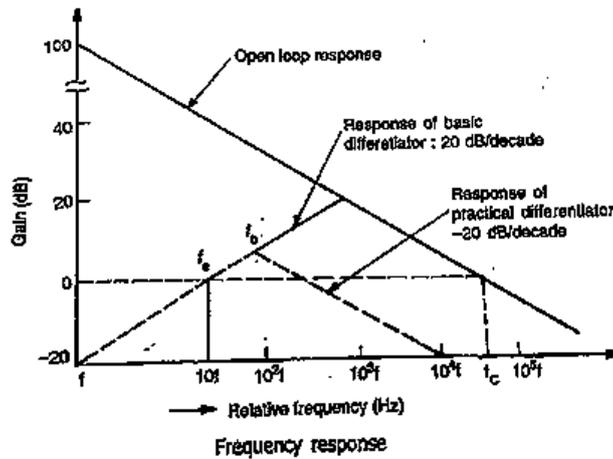
→ This 40 dB/decade change in gain is caused by R_1C_1 and R_fC_f factors.
→ For the basic differentiator of Fig. the frequency response would have increased continuously at the rate of +20 dB/decade even beyond f_b, causing stability problem at high frequency.
→ Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems.
→ The value of f_b should be selected such that,

$$f_a < f_b < f_c$$

where f_c is the unity gain bandwidth of the op-amp in open loop configuration.
→ For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to R_fC_1, that is,

$$T \geq R_fC_1 \to (8)$$

→ It may be noted that for R_fC_1 much greater than R_1C_1 or R_fC_f, equation (5) is reduced to, $V_0/V_i = -sR_fC_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_0 = -R_fC_1\frac{dv_i}{dt} \to (9)$$

→ A resistance R_{comp} (= $R_1 \parallel R_f$) is normally connected to the (+) input terminal to compensate for the input bias circuit.
→ The output waveform for a practical differentiator with a sinusoidal input is given by,

(a) Square wave input

(b) Output for (a)
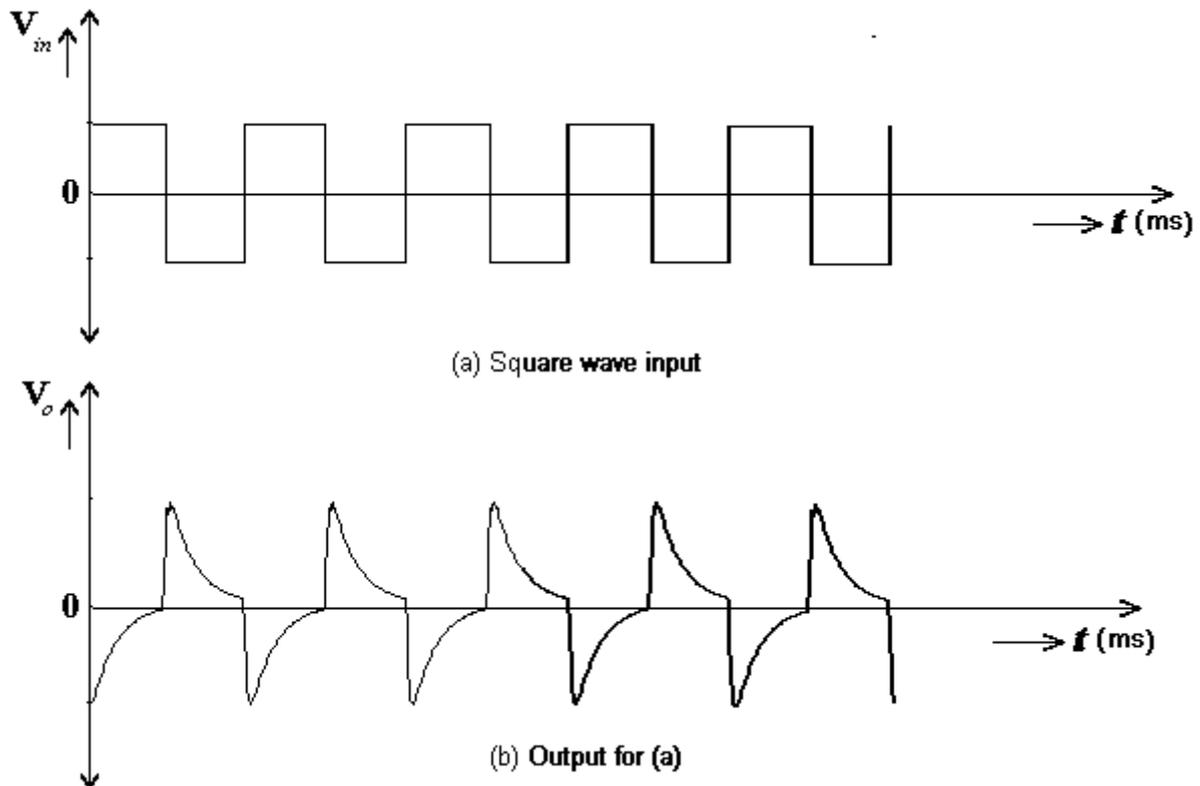
→ A good differentiator may be designed as per the following steps:

❖ Choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 ($<1\mu F$) and then calculate R_f.

❖ Choose $f_b = 10f_a$ (say). Now calculate the values of R_1 and C_f so that $R_1C_1 = R_fC_f$.

6.4 INTEGRATOR

14. With neat diagram explain the working of an OP-AMP based integrator. (8) [APR/MAY 2019]

Or

With the help of circuit diagram show how an OP-AMP is used as an integrator and explain its operation. (8)

Or

With circuit and waveforms explain the application of OP-AMP as an Integrator. (8)

Or

Explain the functions of op-amp as an integrator. Draw the waveforms. (Dec – 14) (4)

6.4 INTEGRATOR:

→ If we interchange the resistor and capacitor of the differentiator we have the circuit of Fig. which as we will see, is an integrator.

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Op-amp Integrator
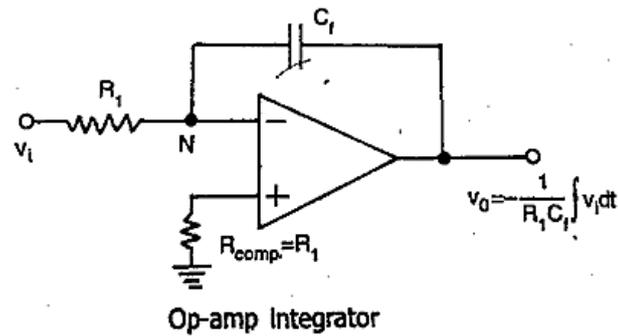
→ The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_f \frac{dv_0}{dt} = 0 \qquad \rightarrow (1)$$

or

$$\frac{dv_0}{dt} = -\frac{1}{R_1 C_f} v_i$$

→ Integrating both sides, we get,

$$\int_0^t dv_0 = -\frac{1}{R_1 C_f} \int_0^t v_i \cdot dt$$

$$v_0(t) = -\frac{1}{R_1 C_f} \int_0^t v_i(t) \cdot dt + v_0(0) \rightarrow (2)$$

Where $v_0(0)$ is the initial output voltage.

→ The circuit, thus provides an output voltage which is proportional to the time integral of the input and $R_1 C_f$ is the time constant of the integrator.

→ It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator.

→ A resistance, $R_{comp} = R$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

→ A simple low pass RC circuit can also work as an integrator when time constant is very large.

→ This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations.

→ However, in the op-amp integrator of Fig. by Miller's theorem, the effective input capacitance becomes Cf (1 – AV) where AV is the gain of the op-amp.

→ The gain AV is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.
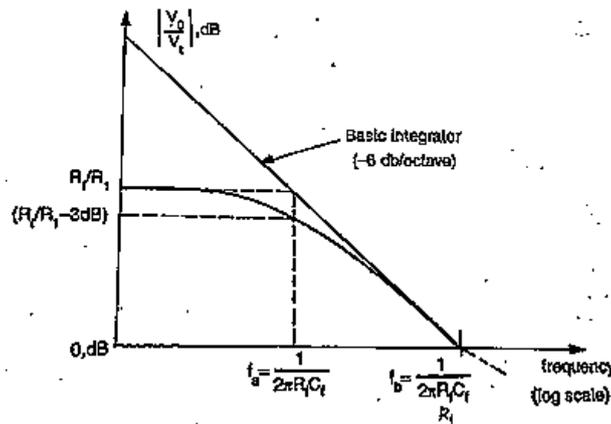
Frequency response of a basic and Lossy Integrator

→ The operation of the integrator can also be studied in the frequency domain. In phasor notation, equation (2) can be written as

$$V_0(s) = -\frac{1}{sR_1C_f}V_i(s) \qquad \rightarrow (3)$$

→ In steady state, put s = jω and we get,

$$V_0(j\omega) = -\frac{1}{j\omega R_1C_f}V_i(j\omega) \qquad \rightarrow (4)$$

→ So, the magnitude of the gain or integrator transfer function is,

$$|A| = \left|\frac{V_0(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1C_f}\right| = \frac{1}{\omega R_1C_f} \rightarrow (5)$$

→ The frequency response or Bode Plot of this basic integrator is shown in Fig.

→ The Bode plot is a straight line of slope – 6B/octave (or equivalently 20dB/decade).

→ The frequency f_b in Fig. is the frequency at which the gain of the integrator is 0 dB and is given by,

$$f_b = \frac{1}{2\pi R_1C_f}$$

→ It can further be seen from equation (5) that at ω = 0, the magnitude of the integrator transfer function is infinite.

→ At dc, the capacitor C_f behaves as an Open circuit and there is no negative feedback.

→ The op-amp thus operates in open loop, resulting in an infinite gain.

→ In practice, of course, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

→ As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator.

→ However, at low frequencies such as at dc (ω ≈ 0), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

6.4.1 Practical Integrator Circuit: (Lossy Integrator)

→ The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_f as shown in Fig.
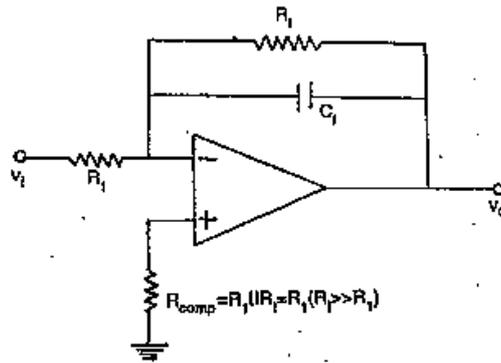
Practical or lossy integrator circuit

→ The parallel combination of R_f and C_f behaves like a practical capacitor which dissipates power unlike an ideal capacitor.

→ For this reason, this circuit is also called a lossy integrator.

→ The resistor R_f limits the low frequency gain to $-R_f/R_1$ (generally $R_f = 10\ R_1$) and thus provides dc stabilization.

6.4.2 Analysis:

→ The nodal equation at the inverting input terminal of the op-amp of Fig. is,

$$\frac{V_i(s)}{R_1} + s\,C_f V_0 + \frac{V_0(s)}{R_f} = 0 \qquad \rightarrow (6)$$

→ from which we have,

$$V_0(s) = -\frac{1}{sR_1 C_f + \frac{R_1}{R_f}} \cdot V_i(s) \qquad \rightarrow (7)$$

→ If R_f is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by,

$$|A| = \left|\frac{V_0}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1{}^2 C_f{}^2 + \frac{R_1^2}{R_f^2}}} = \frac{R_f/R_1}{\sqrt{1 + \left(\omega R_f C_f\right)^2}} \rightarrow (8)$$

→ The Bode plot of the lossy integrator is also shown in Fig. At low frequencies gain is constant at R_f / R_1. The break frequency, $(f = f_a)$ at which the gain is 0.707 (R_f/R_1) (or –3dB below its value of R_f/R_1) is calculated from equation (8) as,

$$\sqrt{1 + \left(\omega R_f C_f\right)^2} = \sqrt{2}$$

→ Solving for $f = f_a$, we get,

$$f_a = \frac{1}{2\pi R_f C_f}$$

→ This is a very important frequency. It tells us where the useful integration range starts.

→ If the input frequency is lower than f_a the circuit acts like a simple inverting amplifier and no integration results.

→ As input frequency equals f_a, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times f_a, then 99% accuracy can result.

→ For a sinusoidal input, the output waveform in an integrator is given as follows:

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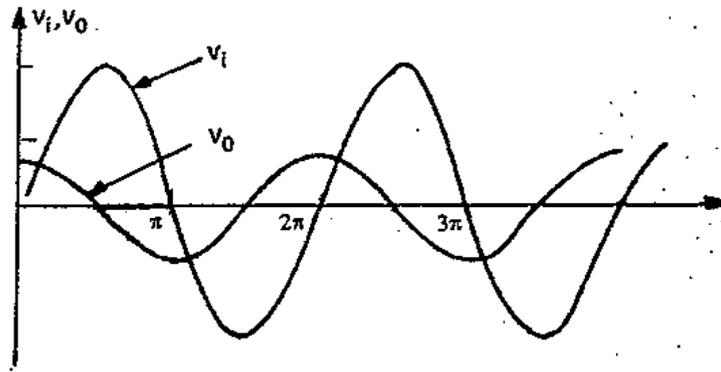
6.5 V-I AND I-V CONVERTERS

**15. Write a note on V-I and I-V converter. (8)**

(or)

Explain voltage to current converter using operational amplifier. (May-15, 17) (8, 5)

6.5.1 V-I CONVERTER: (Trans-conductance Amplifier)

→ In many applications, one may have to convert a voltage signal to a proportional output current.
For this, there are two types of circuits possible.

  ❖ V-I Converter with floating load
  ❖ V-I Converter with grounded load
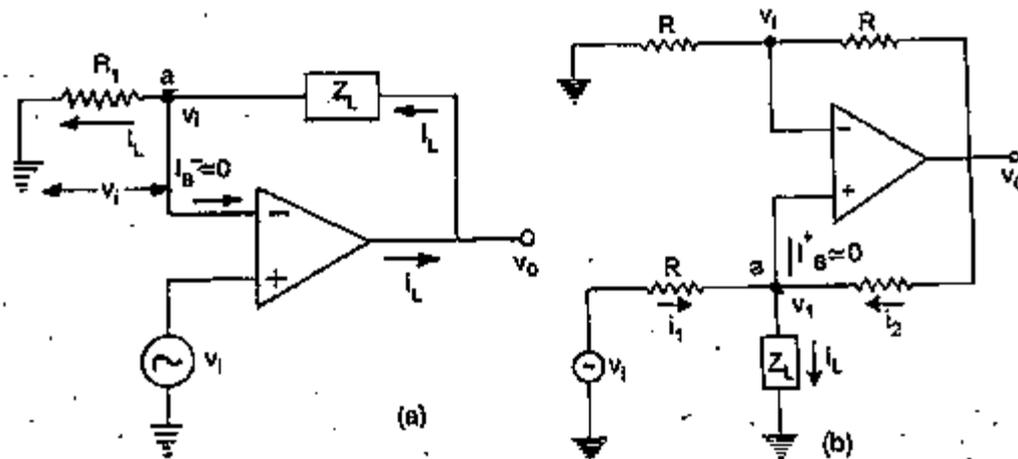
Voltage to current converter with (a) floating load (b) grounded load

→ Figure shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \qquad (as\ I_B^- = 0)$$

or

$$i_L = \frac{v_i}{R_1}$$

→ That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

→ A voltage-to-current converter with grounded load is shown in Fig. Let v_1 be the voltage at node 'a'. Writing KVL, we get,

$$i_1 + i_2 = i_L$$

52

$$\text{or}$$
$$\frac{v_i - v_1}{R} + \frac{v_0 - v_1}{R} = i_L$$
$$\text{or}$$
$$v_i + v_0 - 2v_1 = i_L R$$

Therefore,

$$v_1 = \frac{v_i + v_0 - i_L R}{2}$$

→ Since the op-amp is used in non-inverting mode, the gain of the circuit is $1+R/R = 2$. The output voltage is,

$$v_0 = 2v_1 = v_i + v_0 - i_L R$$

(i.e.)

$$v_i = i_L R$$
$$\text{or}$$
$$i_L = \frac{v_i}{R}$$

→ As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source.

→ A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

6.5.2 I-V CONVERTER: (Trans-resistance Amplifier)

16. Draw and explain the operation of current to voltage converter. (Nov-15) (8)

→ Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light.

→ The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.
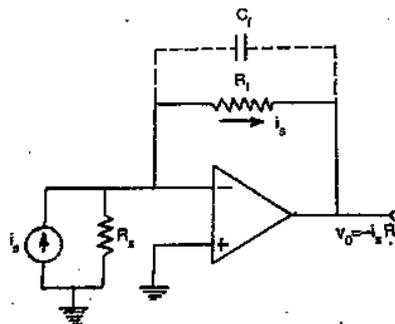
Current to voltage converter

→ Figure shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_S and current i_s flows through the feedback resistor R_f.

→ Thus the output voltage $v_0 = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp.

→ This means that µA741 ($I_B = 3$ nA) can be used to detect lower currents.

→ The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.

UNIT – III

APPLICATIONS OF OP-AMP

Instrumentation amplifier and its applications for transducer bridge – Log and Antilog Amplifiers – analog multiplier & divider, first and second order active filters – comparators – multivibrators – waveform generators – clippers – clampers – peak detector – S/H circuit – D/Aconverter (R – 2R ladder and weighted resistor types) – A/D converters using op amps.

Part – A – 2Mark Questions

1. What is an instrumentation amplifier? (Dec – 14)

→ In many practical circuits it is necessary to amplify low level signals obtained from devices like transducer.

→ The special amplifiers which are basically difference amplifier need for low level signal amplification, having high CMRR, high input impedance and low power consumption are called instrumentation amplifiers.

2. State the important features of an instrumentation amplifier. (May – 05, Dec – 03, l4)

or

What are the basic requirements of a good instrumentation amplifier? [Apr/May 2019]

→ The important features of an instrumentation amplifier are:

1. It is finite, accurate and stable
2. Easy gain adjustment
3. High input impedance
4. Low output impedance
5. High CMRR
6. Low power consumption
7. Low thermal drift
8. High slew rate

3. Draw the circuit diagram of three op-amp instrumentation amplifier.
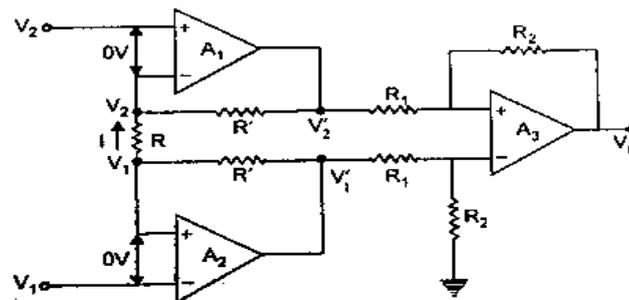
4. Why active guard drive is necessary for an instrumentation amplifier? (May – 12)

→ Practically the common ground bus is shared by variety of circuits.

→ Due to ground loop interference additional voltage drop gets inserted which may cause error in low level measurements.

→ Due to distributed cable capacitances there is degradation of CMRR.

→ The active guard drive eliminates all these problems and hence necessary for an instrumentation amplifier.

5. State any four applications of an instrumentation amplifier.

|	
1. Temperature controller	2. Data acquisition systems
3. Temperature indicator	4. Light intensity meter
5. Analog weight scale	

6. What is comparator? (Dec – 11, May – 12)

→ The open loop op-amp can be used as a comparator.

→ The comparator is a circuit which compares a signal voltage applied at one of the input terminals of the op-amp with a known reference voltage applied at the other input terminal and produces the saturation voltage either high or low, depending on which input is higher.

7. Draw the input and output waveforms of a non-inverting comparator if input is purely sinusoidal.
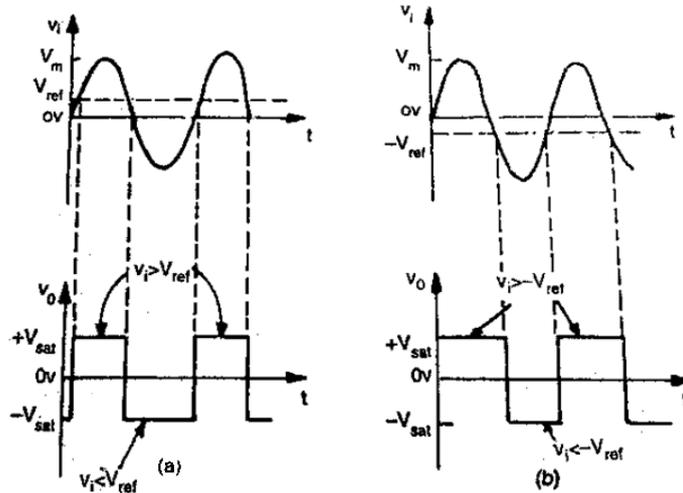
8. Draw the input and output waveforms of inverting comparator if input is purely sinusoidal.
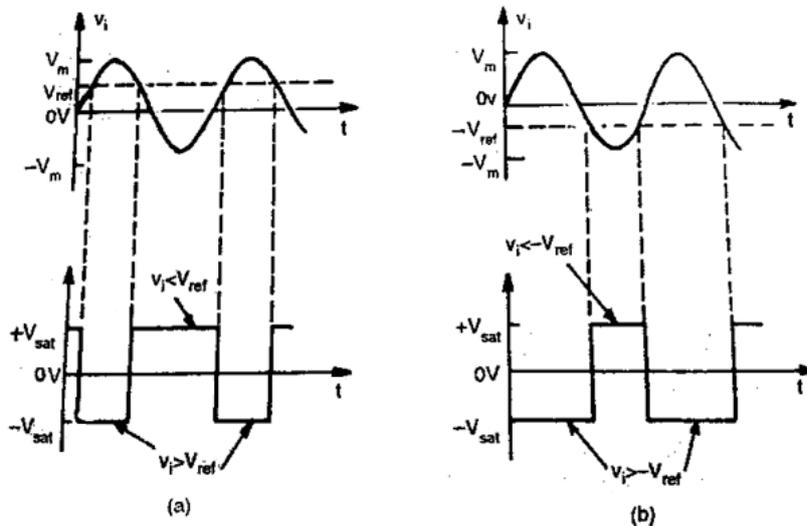
9. List any five characteristics of comparator.

→ While using op-amp as a comparator along with the op-amp parameters following characteristics of a comparator must be considered.

1. Accuracy	2. Logic threshold
3. Response time	4. Positive and negative output level
5. Strobe current	6. Strobe release time

10. What is logic threshold voltage level?

→ It is the voltage level at the output of a comparator at which the connected digital device changes its state.

→ For TTL it is approximately 1.2 V while for CMOS it is 2.5 V.

11. Draw the zero crossing detector and its waveforms. (May – 17)

(a)

(b)
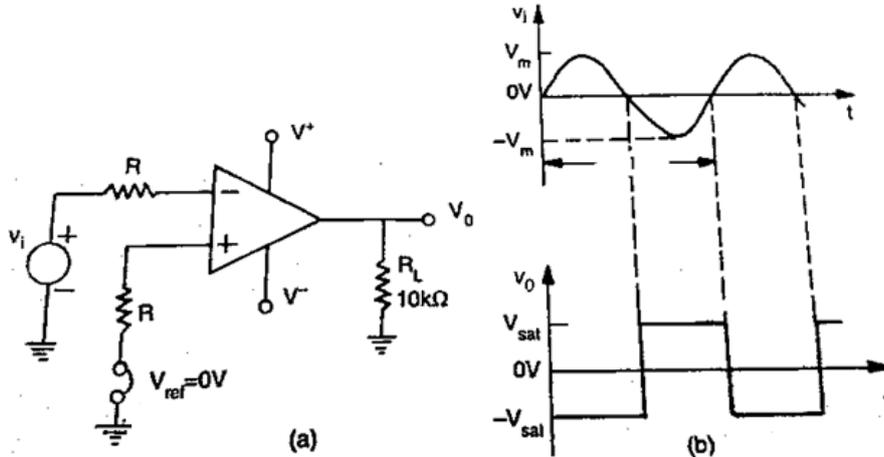
12. List the various applications of a comparator. (May-18)

1. Zero crossing detectors 2. Window detector

3. Level detector4. Schmitt Trigger (Regenerative Comparator)

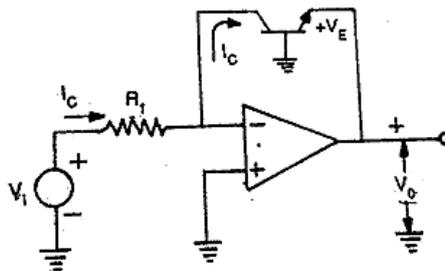## 13. Draw the circuit of inverting Schmitt trigger and its waveforms for sinusoidal input.
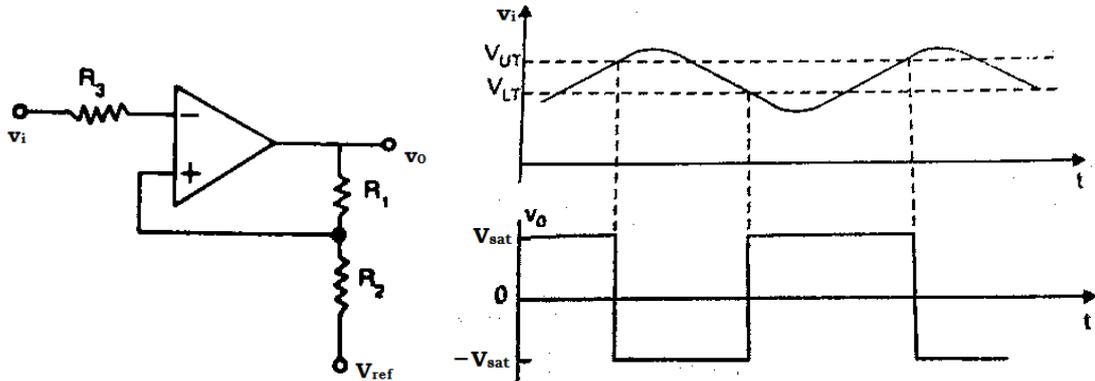
14. What is hysteresis?

→ The graph indicates that once the output changes its state, it remains there indefinitely until the input voltage crosses any of the threshold voltage levels.

→ This is called hysteresis of Schmitt trigger.

→ The hysteresis is also called dead-band or dead-zone.

15. State the three applications of Schmitt trigger. (Dec – 04, May – 05)

1. For eliminating comparator chatter

2. In ON/ OFF controllers

3. For square wave generation

16. Draw the circuit of log amplifier using transistor and write its output expression.

Its output expression is,

3

$$V_0 = -V_T \ln\left[\frac{V_{in}}{V_{ref}}\right]$$

17. What is an antilog amplifier? Draw the circuit diagram of antilog amplifier using transistor and write its output expression. (Dec – 07)

(or)

Draw the circuit of a log amplifier using 2 op-amps. (Nov-15)

(or)

Draw the circuit of antilog OP- AMP amplifier. (Nov/Dec 2019)

→ The circuit which produces the output which is proportional to the antilog of the input is called antilog amplifier.

→ Such op-amp antilog amplifier produces the output proportional to the exponential of the input which is nothing but its antilog.

→ Its output expression is,

$$V_0 = -V_{ref}\, e^{V_{in}/\eta V_T}$$

18. Why temperature compensation is required for the log amplifiers?

→ The reverse saturation current I_Q for the diode changes with temperature.

→ In fact it doubles for every ten degree celsius rise in the temperature.

→ Similarly the emitter saturation current varies significantly from one transistor to other and also with the temperature.

→ Hence it is very difficult to set the term V_{ref} for the circuit.

→ Thus temperature affects the performance and accuracy of the basic logarithmic amplifier circuit.

→ Hence it is must to provide some sort of temperature compensation to reduce the errors.

19. What is a zero crossing detector? (May – 09, 15)

→ A circuit which detects the crossing of zero level by the input signal is called a zero crossing detector.

→ An op-amp comparator is used as a zero crossing detector.

20. What is a filter?

→ A filter is a circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band.

→ The filter circuit using the active elements such as op-amp and transistors along with the passive elements like R, L and C are called active filters.

21. State the advantages of active filters.

or

Why active filters are preferred over passive filters? (Dec – 12)

→ Some of the advantages of active filters are:

1. All the elements along with op-amp can be used in the integrated form. Hence there is reduction in size and weight.

2. In large quantities, the cost of the integrated circuit can be much lower than passive filters.

3. The op-amp gain can be easily controlled in the closed loop fashion hence active filter input signals are not attenuated.

4. Due to flexibility in gain and frequency adjustments, the active filters can be easily tuned.

22. Draw the circuit diagram of first order low pass Butterworth filter. [Apr/May 2019]
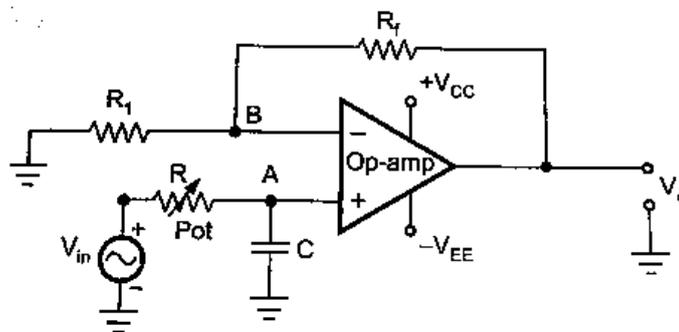
23. What is the rate of decrease in gain for first order and second order low pass Butterworth filters?

→ The rate of decrease in gain for first order Butterworth filter is – 20 dB / decade while for second order low pass Butterworth filter it is – 40 dB / decade.

24. What is frequency scaling?

→ Many times when the filter is designed, practically it is necessary to change its cut-off frequency.

→ The method used to change the cut-off frequency of the filter is called frequency scaling.

25. State the disadvantages of passive filters. (Dec – 03)

→ The disadvantages of passive filters are:

i) Number of elements required is more

ii) The filter gain and frequency adjustments cannot be easily obtained

iii) Causes loading effect

iv) Without inductors, high value of Q cannot be achieved

v) The design procedures are complex

vi) Often exhibits a significant loss

26. What is a sample and hold circuit? (Dec – 07, May – 16)

→ The sample and hold (S/H) circuit samples the value of the input signal in response to a sampling command and hold it at the output until the arrival of the next command is called sample and hold circuit.

→ It samples an analog signal in a very short time in the range of 1 to 10 µs, and holds the sampled signal for an extended period ranging from a few milliseconds to several seconds.

27. What is the need for sample and hold circuit? (Dec – 14)

→ For accurate analog to digital conversion the analog input voltage should be held constant during the conversion cycle.

→ The input voltage is kept constant during conversion time using sample and hold circuit.

28. Draw a sample and hold circuit. (Dec – 05, 14) (May-18)
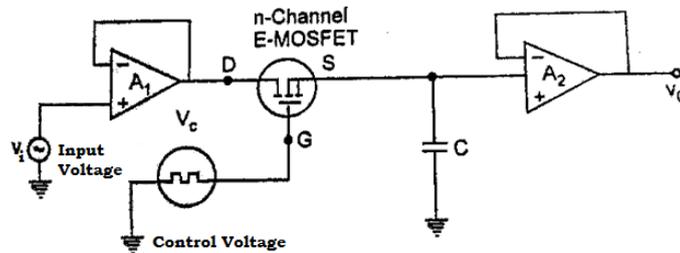
29. What is an analog switch? (Dec – 08)

→ The switch that connects or disconnects the analog input signal to the output is called analog switch.

→ JFET can be used as an analog switch.

30. What are the advantages or uses of sample and hold circuits? (Nov-17)

1. The primary use of the sample and hold circuit is to hold the sampled analog input voltage constant during conversion time of A/D converter.
2. In case of multichannel ADCs, synchronization can be achieved by sampling signals from all channels at the same time.
3. It also reduces the crosstalk in the multiplexer.

31. State the applications of sample and hold circuits. (Dec – 07)

→ The applications of sample and hold circuits are:
1. Digital Interfacing
2. Analog to Digital converter circuits
3. Pulse modulation systems
4. Reset-stabilised op-amps
5. Analog de-multiplexers

32. What are A/D and D/A converters?

→ The circuit that performs conversion of analog signal into digital signal is called **analog to digital (A/D) converter**.

→ On the other hand, the circuit that performs conversion of digital signal into analog signal is called **digital to analog (D/A) converter**.

33. Define resolution of a D/A converter. (May – 05, 10, Dec – 08, 10, 11)

→ Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC,

$$Resolution = 2^n$$

→ Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC,

$$Resolution = \frac{V_{OFS}}{2^n - 1}$$

34. Find the resolution of a 12-bit D/A converter. (May – 09)

$$Resolution = 2^n = 2^{12} = 4096$$
n is the number of bits

35. Define accuracy of D/A converter. (May – 11)

→ It is a comparison of actual output voltage with expected output voltage.

→ It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst, ± ½ of its LSB.

36. Define monotonicity with respect to D/A converter. (May – 04)

→ A converter is said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.

37. Define conversion time of DAC. (Dec – 10)

→ It is defined as the time required for conversion of analog signal into its digital equivalent.

38. Define settling time. (May – 12)

→ It is defined as the time required for the output of the DAC to settle to within ± ½ LSB of the final value for a given digital input i.e. zero to full scale.

39. What are the specifications of DAC? Give the basic types of DAC.

→ The specifications of D/A converter are:

      1. Accuracy   2. Resolution   3. Offset

      4. Linearity Error   5. Conversion Time   6. Monotonicity

→ The basic types of D/A converter are:

      1. Binary weighted resistor DAC

      2. R-2R ladder DAC

40. What are the drawbacks of binary weighted DAC?

→ The drawbacks of binary weighted DAC are:

      1. Wide range of register values is required.

      2. It is impractical to fabricate large values of resistors and for smaller values of resistors, the loading effect may occur. This limits the resolution of binary weighted resistor DAC.

41. State the advantages of R-2R ladder DAC.(or)

Why is the R-2R ladder network DAC better than weighted resistor DAC? (Dec – 03)

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R-2R values.
3. In inverted R-2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

42. Compare and contrast binary ladder and R-2R ladder DAC. (Dec – 10)

Binary Ladder	R-2R Ladder
It uses resistor scaling and common voltage reference.	It uses voltage scaling and identical resistors.
It uses multiple resistor values with a wide range of resistor values. For 8-bit DAC, the resistors required are 2^1R, 2^2R, 2^3R . . . and 2^8R. Therefore, the largest resistor is 128 times the smallest one.	It uses only two resistor values.
It is impractical to fabricate large values of resistors and for smaller values of resistors, the loading effect may occur. Thus it is difficult to fabricate binary weighted resistor DAC.	Since it uses only two resistor values, it is easy to fabricate R-2R ladder DAC.

43. What output voltage will be produced by a 4-bit D/A converter whose output range is 0 V to 10 V and whose input binary number is 0110?

$$Resolution = \frac{V_{OFS}}{2^n - 1} = \frac{10}{2^4 - 1} = 0.667 \, V$$

7

$$V_0 = 0.667 \times (0110)_2 = 0.667 \times 6 = 4V$$

44. List the basic A/D conversion techniques.

$\rightarrow$ The basic A/ D conversion techniques are:

      1. Single ramp at single slope   2. Dual slope

      3. Successive approximation   4. Flash

45. What is quantization noise? (May – 03)

$\rightarrow$ The coding of different analog signal values with the same digital word, depending on the intrinsic finite resolution of a converter implies an error called the quantization error or quantization noise.

$\rightarrow$ It is defined as the difference between the transfer characteristics of a converter with finite resolution and that of a converter with an infinite resolution.

46. List the advantages of dual slope ADC.   **(or)**

Give the advantages of integrating type ADC. (May – 10, Dec – 10)

$\rightarrow$ The advantages of dual slope ADC are:

      1. It is highly accurate   2. Its cost is low

      3. It is immune to temperature caused variations in R_1 and C_1

47. Which type of ADC is used in all digital voltmeters? (Dec – 03)

$\rightarrow$ Dual slope A/ D converter

48. State the reason for keeping the integrating time in the dual slope analog to digital converter equal to that of mains supply period. (May – 07)

$\rightarrow$ Reason for keeping the integrating time in the dual slope analog to digital converter equal to that of main supply period is to obtain excellent noise rejection as noise and superimposed power supply hum are averaged out during the process of integration.

49. State the disadvantages of counter type ADC. (May-18)

$\rightarrow$ The disadvantages of counter type ADC are:

     ➢ It is necessary to give enough time for DAC conversion and comparator to respond. Therefore, there is a limitation on the clock frequency. As clock frequency is low, the speed of conversion is less.

     ➢ Conversion time is not constant. It increases with increase in input voltage. In other words, we can say that conversion time is high at high input voltage.

50. Which is the fastest A/D converter? Give reason. (Dec – 06, 09, 11, May – 11,17)

$\rightarrow$ Flash ADC is the fastest ADC technique since its output is available immediately after the time equal to propagation delay of a comparator.

51. What is the main drawback of dual slope ADC? (May – 12)

$\rightarrow$ The conversion time of dual slope ADC is high. This is the main drawback of dual slope ADC.

52. What is a mono stable multi vibrator circuit? State the expression for its pulse width.

$\rightarrow$ The circuit which produces a single pulse of specified duration in response to each external trigger signal is called mono stable multi vibrator circuit.

$\rightarrow$ It has only one stable state and it is also called one shot mutivibrator.

$$Pulse\ width, T = RC\ \ln\left[\frac{1 + V_{D1}/V_{sat}}{1 - \beta}\right]$$

53. What is an as table multivibrator circuit? State the expression for its frequency of oscillation.

$\rightarrow$ The circuit which has two quasi-stable states and which oscillates between these two states without application of the trigger signal is called an astable multivibrator circuit.

$\rightarrow$ It is also called free running multivibrator.
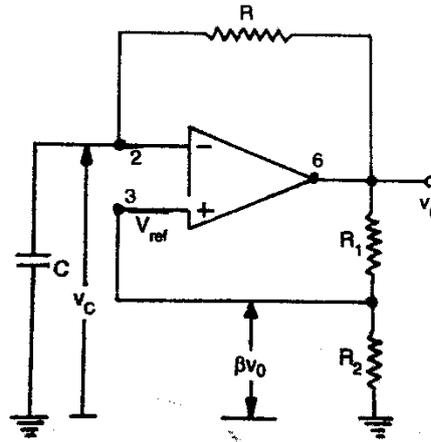
$$Frequency, f = \frac{1}{2R_f C \ln\left(\frac{2R_1+R_2}{R_2}\right)}$$

54. State the applications of mono stable multivibrator.

        1. Frequency divider   2. Missing pulse detector

        3. Pulse width modulation   4. Pulse position modulation

        5. Linear ramp generator

55. State the applications of an astable multivibrator.

        1. Square wave generator   2. FSK generator

        3. Voltage controlled oscillator

56. State the Barkhausen conditions required for the oscillations. (Dec – 05)

$\rightarrow$ The conditions required for producing the oscillations are given by the Barkhausen criterion which states that:

    1. The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0^0 or 360^0, or of course an integral multiple of 2π radians.

    2. The magnitude of the product of the open loop gain of the amplifier (A) and the feedback factor β is unity i.e. $|A\beta| = 1$.

57. A dual slope ADC has a reference voltage of a 100 mV and t_1 = 83.33 ms. Find t_2 if v_i = 200 mV. (Dec – 09)

    We know that,

$$t_2 = \left(\frac{v_i}{v_R}\right)t_1$$

$$\therefore \; t_2 = \left(\frac{200}{100}\right)(83.33) = \mathbf{166.6 \; ms}$$

58. For n-bit flash type A/D converter what is the number of comparators required and write the disadvantages of that type of a converter. (Dec – 04) (May-15)

$\rightarrow$ Number of comparators required = $2^n - 1$

$\rightarrow$ The disadvantages of flash type A/D converters are:

    1. Large number of comparators is required as n increases. Thus ADCs are restricted to 8 bits.

    2. Cost is high

    3. Less Accurate

59. What is meant by cut off frequency of a high pass filter and how it is found out in a first order high pass filter?

→ The frequency at which the gain is 0.707 times the gain of band pass filter is called **low cut-off frequency** and is denoted as f_L.

where,

$$f_L = \frac{1}{2\pi RC}$$

60. Where do we use successive approximating type ADC?

→ Successive Approximation type ADC is used in Data acquisition systems.

61. What are the applications of Peak Detectors? (Dec – 12)

→ Peak Detectors find application in

        1. Test and Measurement Instrumentation

        2. Amplitude Modulation Communication

62. Draw the circuit of a Positive Clipper. (Dec – 14)
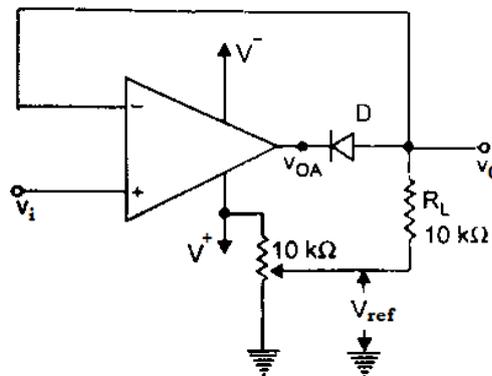
63. Calculate the value of LSB, MSB and full scale output for an 8- bit DAC for 0 to 12V range. (Nov-15)

LSB= 1/ 2^8 = 1/256

For 12V range LSB= 12/256=46mV

MSB=1/2*(full scale) = ½*(12V) = 6V

Full scale output= (full scale voltage-1 LSB)

= 12V- 0.046V = 11.954V

64. List the applications of clipper and clamper circuits. (Nov-17)

- Clipper and Clamper are widely used in analog television receivers and FM transmitters.

1. **INSTRUMENTATION AMPLIFIER AND ITS APPLICATIONS OF TRANSDUCER BRIDGE**

1. Draw the circuit of instrumentation amplifier and derive the expression for output voltage for in it. Also write the advantages of instrumentation amplifier. (16)

(or)

Explain the working of instrumentation amplifier. (May-15) (8)

1. **INSTRUMENTATION AMPLIFIER:**

→ In a number of industrial and consumer applications, one is required to measure and control physical quantities.

→ Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc.

→ These physical quantities are usually measured with the help of transducers.

→ The output of transducer has to be amplified so that it can drive the indicator or display system.

→ This function is performed by an instrumentation amplifier.

→ The important features of an instrumentation amplifier are:

> ➢ High gain accuracy
> ➢ High CMRR
> ➢ High gain stability with low temperature coefficient
> ➢ Low d.c. offset
> ➢ Low output impedance

→ Consider the basic differential amplifier shown in Fig. 1.
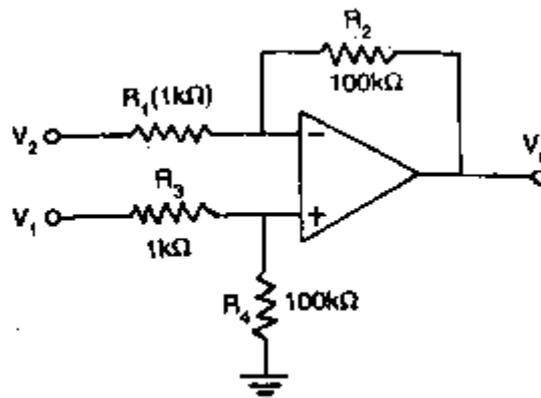
Fig. 3.1 Differential amplifier using single op-amp

→ It can be easily seen that the output voltage V_0 is given by,

$$V_0 = -\frac{R_2}{R_1} V_2 + \frac{1}{1 + \frac{R_3}{R_4}} V_1 \left(1 + \frac{R_2}{R_1} \right)$$

or

$$V_0 = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1 + \frac{R_3}{R_4}}\left(\frac{R_1}{R_2} + 1\right)V_1\right]$$

$\rightarrow$ For $R_1/R_2 = R_3/R_4$, we obtain

$$V_0 = \frac{R_2}{R_1}(V_1 - V_2)$$

$\rightarrow$ In the circuit of Fig. 1, source V_1 sees an input impedance $= R_3 + R_4(101\ k\Omega)$ and the impedance seen by source V_2 is only R_1 (1 kΩ).

$\rightarrow$ This low impedance may load the signal source heavily. Therefore, high resistance buffer is used after each input to avoid this loading effect as shown in Fig. 2.
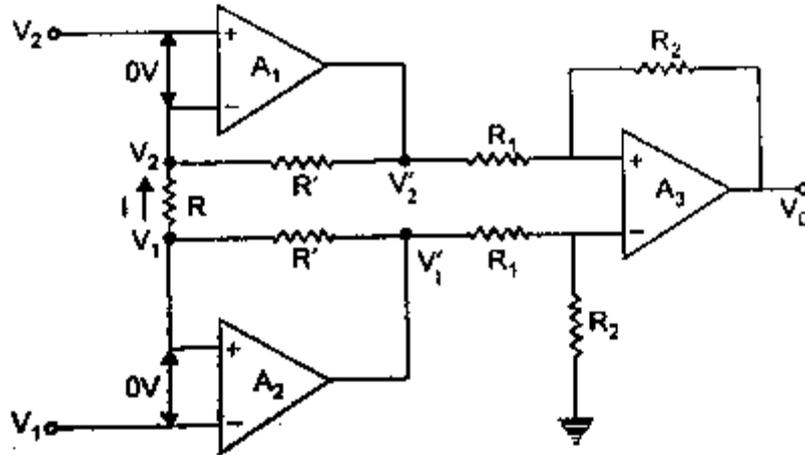
Fig. 3.2An improved Instrumentation amplifier

$\rightarrow$ The op-amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$, that is, under common mode condition, the voltage across R will be zero.

$\rightarrow$ As no current flows through R and R' the non-inverting amplifier A_1 acts as voltage follower so its output $V_2' = V_2$.

$\rightarrow$ Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$.

$\rightarrow$ However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2' - V_1') > (V_2 - V_1)$.

$\rightarrow$ Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of Fig. 1.

$\rightarrow$ The output voltage V_0 can be calculated as follows:

$\rightarrow$ The voltage at the (+) input terminal of op-amp A_3 is,

$$\frac{R_2 V_1'}{R_1 + R_2}$$

$\rightarrow$ Using superposition theorem, we have,

$$V_0 = -\frac{R_2}{R_1}V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$

$$V_0 = \frac{R_2}{R_1}\left(V_1' - V_2'\right)$$

$\rightarrow$ Since, no current flows into op-amp, the current I flowing (upwards) in R is,

$$I = (V_1 - V_2)/R$$

and passes through the resistor R'.

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1$$

12

and

$$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2$$

→ Putting the values of V_1' and V_2' in V_0 equation, we get,

$$V_0 = \frac{R_2}{R_1}\left(\frac{R'}{R}(V_1 - V_2) + V_1 - \left(-\frac{R'}{R}(V_1 - V_2) + V_2\right)\right)$$

$$V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

or

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2)$$

→ The difference gain of this instrumentation amplifier can be varied by using a variable resistance R.
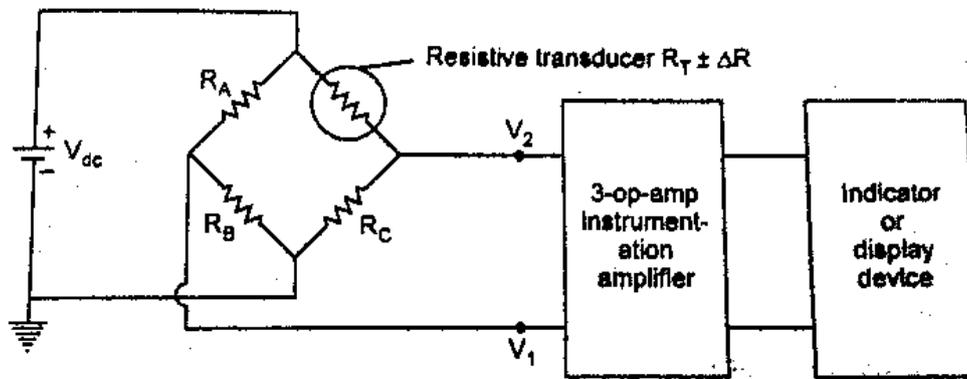
Fig. 3.3 Instrumentation amplifier using Transducer Bridge

→ Fig. 3 shows a differential instrumentation amplifier using Transducer Bridge.
→ The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.
→ The bridge is initially balanced by a d.c. supply voltage V_{dc} so that $V_1 = V_2$.
→ As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$).
→ This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

PROBLEM:

2. **Find the following for the given op- amp differential amplifier: (i) the gain of the amplifier (ii) the input resistance (iii) output voltage. When the input are 1sin (2000t)V, 1.2 sin(2000t)V and R1=R3=1.2KΩ, R2=R4= 22KΩ. (Apr/May 2019) 13 marks**
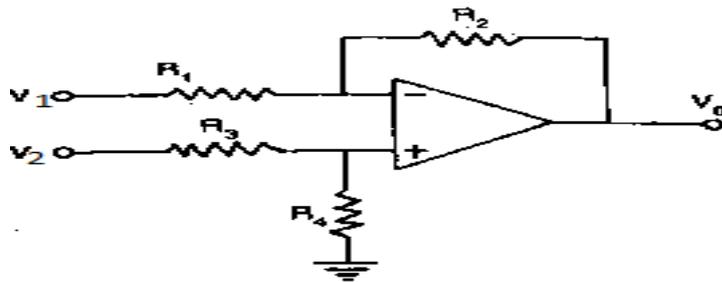
Solution:
Given Parameters:
$V_1 = 1\sin(2000t)$ V; $V_2 = 1.2\sin(2000t)$
$R_1 = R_3 = 1.2$ KΩ
$R_2 = R_4 = 22$ KΩ

(i) Output voltage
   $V_0 = (R_2/R_1)(V_1 - V_2)$
   $= (22 \text{ K}\Omega / 1.2 \text{ K}\Omega)(1.2 - 1)$
   $V_0 = 3.67$ V
   $V_{in} = V_1 + V_2 = (1 + 1.2)$
   $= 2.2$V

(ii) Gain of the amplifier
   $A_V = V_0/V_{in}$
   $= 3.67/2.2$
   $= 1.67$ V

(iii) Input resistance
   For V_1
   Input resistance $V_i = R_1 = 1.2$ KΩ
   For V_2
   Input resistance $V_i = R_3 + R_4 = (1.2 + 22)$
   $= 23.2$ KΩ

2. LOG AND ANTILOG AMPLIFIERS

3. **With circuit diagram explain the working of log and anti-log amplifiers. (Dec –14)**

2. LOG AND ANTILOG AMPLIFIER:

→ There are several applications of log and antilog amplifiers.

→ Antilog computation may require functions such as lnx, log x or sinh x.

→ These can be performed continuously with log-amps.

→ One would like to have direct dB display on digital voltmeter and spectrum analyser.

→ Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

2.1 Log Amplifier:

→ The fundamental log-amp circuit is shown in Fig. 4 where a grounded base transistor is placed in the feedback path.

→ Since the collector is held at virtual ground and the base is also grounded the transistor's voltage-current relationship becomes that of a diode and is given by,
$$I_E = I_S\left(e^{qV_E/kT} - 1\right)$$

→ Since, $I_C = I_E$ for a grounded base transistor,
$$I_C = I_S\left(e^{qV_E/kT} - 1\right)$$
$$I_S = emitter\ saturation\ current \approx 10^{-13}A$$
$$k = Boltzmann's\ constant$$
$$T = absolute\ temperature\ (in\ {}^0K)$$

Therefore,

$$\frac{I_C}{I_S} = \left(e^{qV_E/kT} - 1\right)$$

or

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1$$

$$\approx \frac{I_C}{I_S}$$

as $I_s \approx 10^{-13}$ A, $I_C \gg I_S$

$\rightarrow$ Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$
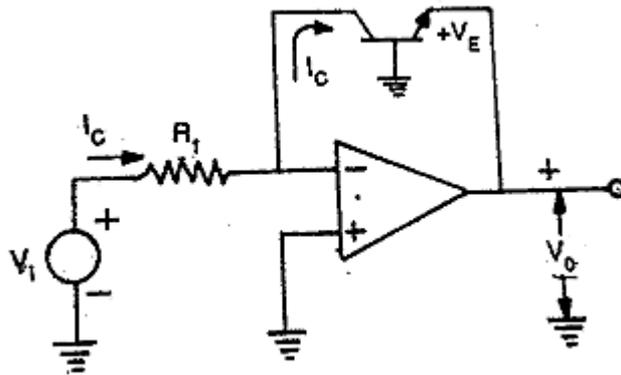
Fig. 3.4 Fundamental log-amp circuit

Also in Fig. 3.4,

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_0$$

so,

$$V_0 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

where,

$$V_{ref} = R_1 I_S$$

$\rightarrow$ The output voltage is thus proportional to the logarithm of input voltage.

$\rightarrow$ Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling.

$$\log_{10} X = 0.4343 \ln X$$

$\rightarrow$ The circuit, however, has one problem. The emitter saturation current I_S varies from transistor to transistor and with temperature.

$\rightarrow$ Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 5.
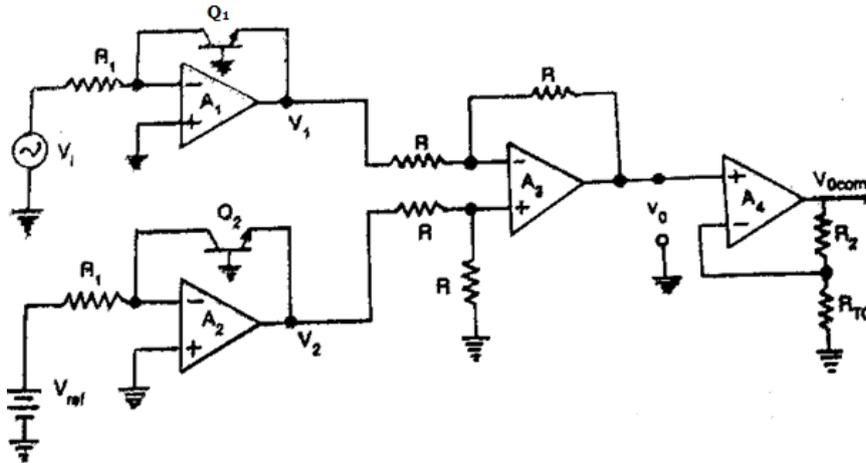
Fig. 3.5 Log-amp with saturation current and temperature compensation

→ The input is applied to one log-amp, while a reference voltage is applied to another log-amp.

→ The two transistors are integrated close together in the same silicon wafer.

→ This provides a close match of saturation currents and ensures good thermal tracking.

Assume, $\qquad I_{S1} = I_{S2} = I_S$

and then,

$$V_1 = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_S}\right)$$

and

$$V_2 = -\frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

Now,

$$V_0 = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_S}\right) - \ln\left(\frac{V_{ref}}{R_1 I_S}\right)\right]$$

or

$$V_0 = \frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

→ Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed.

→ The voltage V_0 is still dependent upon temperature and is directly proportional to T.

→ This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$.

→ Now, the output voltage is,

$$V_{0\,comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

→ where, R_{TC} is a temperature sensitive resistance with a positive co-efficient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

→ The circuit in Fig.3.5 requires four op-amps, and becomes expensive if FET op-amps are used for precision.

→ The same output (with an inversion) can be obtained by the circuit of Fig. 6 using two op-amps only.
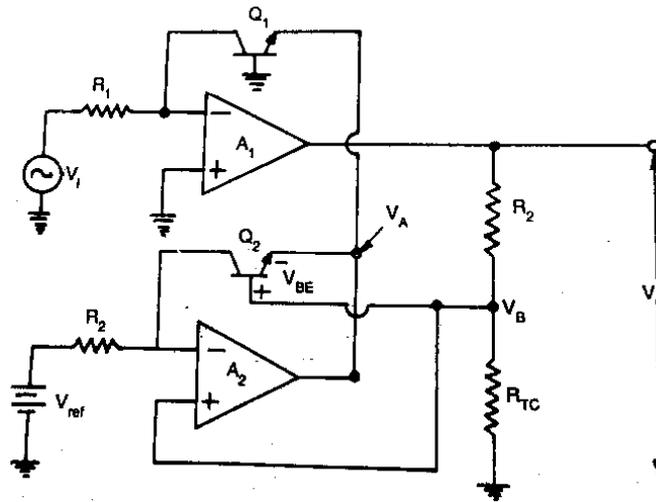
Fig. 3.6 Log-amp using two op-amps only

2.2 Antilog Amplifier:

→ The circuit is shown in Fig.3.7.
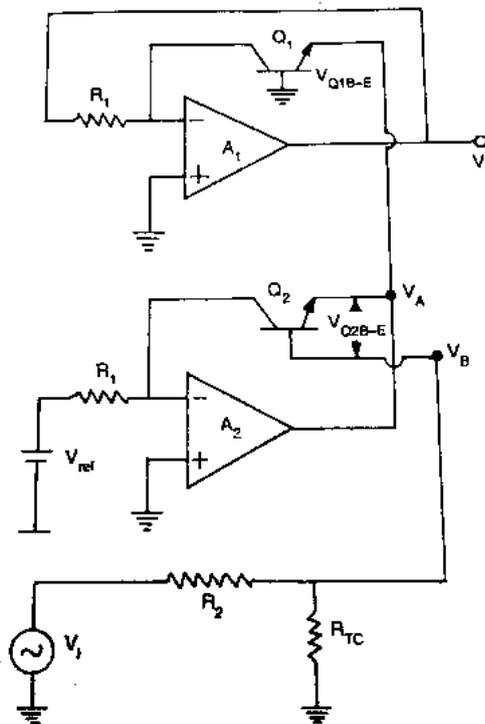
Fig. 3.7 Antilog amplifier

→ The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2.

→ The output V_0 of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1.

→ The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\,B-E} = \frac{kT}{q} ln\left(\frac{V_0}{R_1 I_S}\right)$$

and

$$V_{Q2\,B-E} = \frac{kT}{q} ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

→ Since the base of Q_1 is tied to ground, we get,

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$$V_A = -V_{Q1\,B-E} = -\frac{kT}{q} ln\left(\frac{V_0}{R_1 I_S}\right)$$

→ The base voltage V_B of Q_2 is,

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

→ The voltage at the emitter of Q_2 is,

$$V_{Q2\,E} = V_B + V_{Q2\,E-B}$$

or

$$V_{Q2\,E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

→ But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\,E}$$

or

$$-\frac{kT}{q} ln\left(\frac{V_0}{R_1 I_S}\right) = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

or

$$\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = -\frac{kT}{q} \left(ln\left(\frac{V_0}{R_1 I_S}\right) - ln\left(\frac{V_{ref}}{R_1 I_S}\right)\right)$$

or

$$-\frac{q}{kT} \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = ln\left(\frac{V_0}{V_{ref}}\right)$$

→ Changing natural log to $\log_{10}$ we get,

$$-0.4343 \left(\frac{q}{kT}\right) \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = 0.4343 \times ln\left(\frac{V_0}{V_{ref}}\right)$$

or

$$-K' V_i = \log_{10}\left(\frac{V_0}{V_{ref}}\right)$$

or

$$\frac{V_0}{V_{ref}} = 10^{-K' V_i}$$

or

$$V_0 = V_{ref}\left(10^{-K' V_i}\right)$$

where, $$K' = 0.4343 \left(\frac{q}{kT}\right) \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

→ Hence an increase of input by one volt causes the output to decrease by a decade.

4. <u>ANALOG MULTIPLIER AND VOLTAGE DIVIDER</u>

4.1 ANALOG MULTIPLIER

4. Explain the op-amp application as analog multiplier circuit.

→ A multiplier is a circuit which produces output that is the product of two inputs applied.

→ A circuit which performs multiplication of two analog voltages is called as analog multiplier.

→ If V_1 and V_2 were the two input analog voltages applied, then the output voltage V_0 is given as,

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$V_0 = k\, V_1\, V_2$

Where, k – scaling factor

→ The use of a scaling factor k is to avoid the saturating output.

→ This is because; the product of two input voltages with moderate value could cause the output to reach saturation.

→ In such a situation, it may become impossible to measure the desired product output V_0.

→ The above expression for V_0 is the ideal output voltage. They are
   (i)   Input signal offset (φ_1 & φ_2)
   (ii)   Error in scaling factor k (e)
   (iii)   Output signal offset (φ_0)

With all these parameters, the output of a practical multiplier is given as V_0 defined by,

$$V_0 = \frac{(V_1 + \varphi_1)(V_2 + \varphi_2)}{10^X(1 + e)} + \varphi_0$$

Note that x can be any integer or fractional value.

4.2 Voltage Divider

5. **Explain the op-amp application as voltage divider circuit.**

→ Voltage divider can be implemented by connecting a multiplier in the feedback loop of an op-amp as shown here in figure below.

→ V_{num} is the numerator voltage and V_{den} is the denominator voltage.

→ Note that node 'a' is at virtual ground and other end of R_c is physically grounded.

→ From the diagram,

   $i_1 + i_2 = 0$ and substituting $i_1 = \frac{V_{num}}{R}$; $i_2 = \frac{V_{om}}{R}$

$$\frac{V_{num}}{R} + \frac{V_{om}}{R} = 0$$

   & $V_{om} = k\, V_{OA} V_{den} = -V_{num}$

   [Where V_{om} is output of multiplier with two inputs V_{OA} and V_{den}]

$$V_{OA} = \frac{-V_{num}}{KV_{den}}$$

→ K is the scale factor. Thus output V_{OA} from op-amp is the divided voltage.
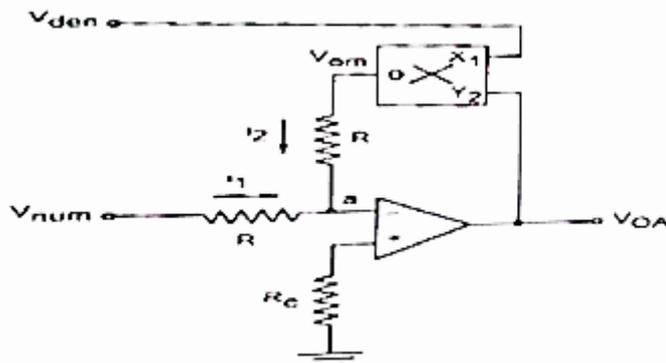
6. Draw the circuit of a first order Butterworth low pass filter and derive its transfer function.

5.1 FIRST ORDER LOW PASS BUTTER-WORTH FILTER:

→ The first order low pass Butterworth filter is realised by R-C circuit used along with an op-amp, used in the non-inverting configuration.

→ The circuit diagram is shown in Fig. 8.
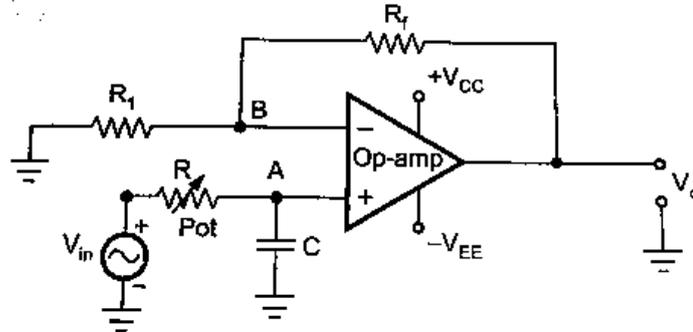
Fig. 3.8 First Order Low Pass Butterworth Filter

→ This is also called **one pole low pass Butterworth filter**.

→ The resistances R_f and R_1 decide the gain of the filter in the pass band.

5.1.1 Analysis of the Filter Circuit:

→ The impedance of the capacitor C is $-jX_C$ where X_C is the capacitive reactance given by,

$$X_C = \frac{1}{2\pi f C}$$

→ By the potential divider rule, the voltage at the non-inverting input terminal A which is the voltage across capacitor C is given by,

$$V_A = \frac{-jX_C}{R - jX_C} \cdot V_{in}$$

$$\therefore \quad V_A = \frac{-j\left(\frac{1}{2\pi f C}\right)}{R - j\left(\frac{1}{2\pi f C}\right)} \cdot V_{in} = \frac{-j}{2\pi f RC - j} \cdot V_{in} = \frac{V_{in}}{1 - \frac{2\pi f RC}{j}}$$

but $-j = 1/j$ and $-1/j = j$

$$\therefore \quad V_A = \frac{V_{in}}{1 + j2\pi f RC}$$

→ As the op-amp is in the non-inverting configuration,

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_A$$

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) \cdot \frac{V_{in}}{1 + j2\pi f RC}$$

i.e.

$$\frac{V_0}{V_{in}} = \frac{A_F}{1 + j\left(\frac{f}{f_H}\right)}$$

where, $\quad A_F = \left(1 + \frac{R_f}{R_1}\right) = Gain\ of\ filter\ in\ pass\ band$

$$f_H = \frac{1}{2\pi f C} = High\ cut - off\ frequency\ of\ filter$$

and

$$f = Operating\ frequency$$

→ The V_0 / V_{in} is the transfer function of the filter and can be expressed in the polar form as,

$$\frac{V_0}{V_{in}} = \left|\frac{V_0}{V_{in}}\right| < \varphi$$

where,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

and

$$\varphi = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

The phase angle Φ is in degrees.

→ The transfer function equation describes the behaviour of the low pass filter.

   ➢ At very low frequencies, $f < f_H$

   $$\left|\frac{V_0}{V_{in}}\right| = A_F\ i.e.\ constant$$

   ➢ At $f = f_H$,

   $$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707 A_F\ i.e.\ 3\ dB\ down\ to\ the\ level\ of\ A_F$$

   ➢ At $f > f_H$

   $$\left|\frac{V_0}{V_{in}}\right| < A_F$$

→ Thus for the range of frequencies, $0 < f < f_H$, the gain is almost constant equal to f_H which is high cut-off frequencies.

→ At $f = f_H$, gain reduces to 0.707 A_F i.e. 3 dB down from A_F and as the frequency increases than f_H, the gain decreases at a rate of 20 dB / decade.

→ The rate 20 dB / decade mean decrease of 20 dB in gain per 10 times change in frequency.

→ The same rate can be expressed as 6 dB / octave i.e. decrease of 6 dB per two times change in the frequency.

→ The frequency f_H is called **cut off frequency**, **break frequency**, **-3 dB frequency** or **corner frequency**.

→ The frequency response is shown in the Fig. 9.
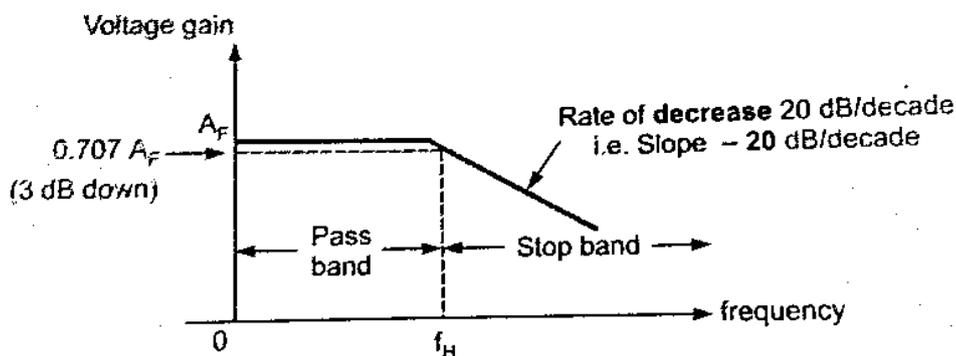
Fig. 3.9 Frequency Response

5.1.2 Design steps:

The design steps for the first order low pass Butterworth filter are,

   ➢ Choose the cut-off frequency, f_H.

➢ Choose the capacitance C usually between 0.001 and 1µF. Generally, it is selected as 1µF or less than that. For better performance, Mylar or Tantalum capacitors are selected.

➢ Now, for the RC circuit, $f_H = \frac{1}{2\pi f C}$

➢ Hence, as f_H and C are known, calculate the value of R.

➢ The resistance R_f and R_1 can be selected depending on the required gain in the pass band. $A_F = \left(1 + \frac{R_f}{R_1}\right)$

5.2 <u>SECOND ORDER LOW PASS BUTTERWORTH FILTER:</u>

7. Draw the circuit of a second order Butterworth low pass filter and derive its transfer function. (Nov-17) (16, 13)

(or)

Design a second order butter worth low pass filter having upper cut-off frequency of 1 kHz. (Nov-15) (12)

→ The practical response of the filter must be very close to an ideal one.

→ In case of low pass filter, it is always desirable that the gain rolls off very fast after the cut off frequency, in the stop band.

→ In case of first order filter, the gain rolls off at a rate of 40 dB / decade.

→ Thus, the slope of the frequency response after f = f_H is – 40 dB / decade, for a second order low pass filter.

→ A first order filter can be converted to second order type using an additional RC network as shown in the fig.3.10.
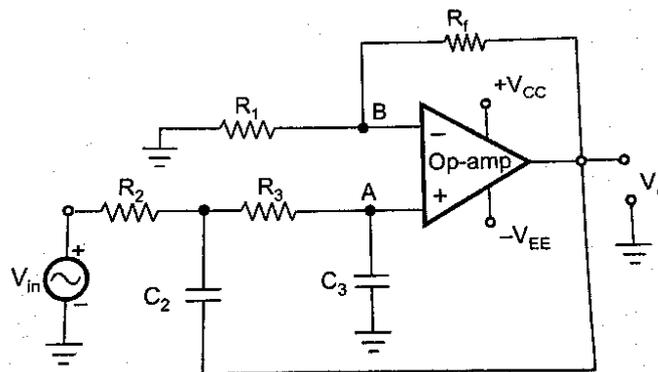
Fig. 3.10 Second Order Low Pass Butterworth Filter

→ The cut off frequency f_H for the filter is now decided by R_2, C_2, R_3, and C_3.

→ The gain of the filter is as usual decided by op-amp i.e. the resistance R_1 and R_f.

5.2.1 <u>Analysis of the Filter circuit:</u>

→ For deriving the expression for the cut off frequency, let us use the Laplace transform method.

→ The input RC network can be represented in the Laplace domain as shown in Fig. 3.11

Now,

$$I_1 = I_2 + I_3 \qquad\qquad \to (1)$$

i.e.

$$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_0}{\left(\frac{1}{sC_2}\right)} + \frac{V_1 - V_A}{R_3} \qquad \rightarrow (2)$$
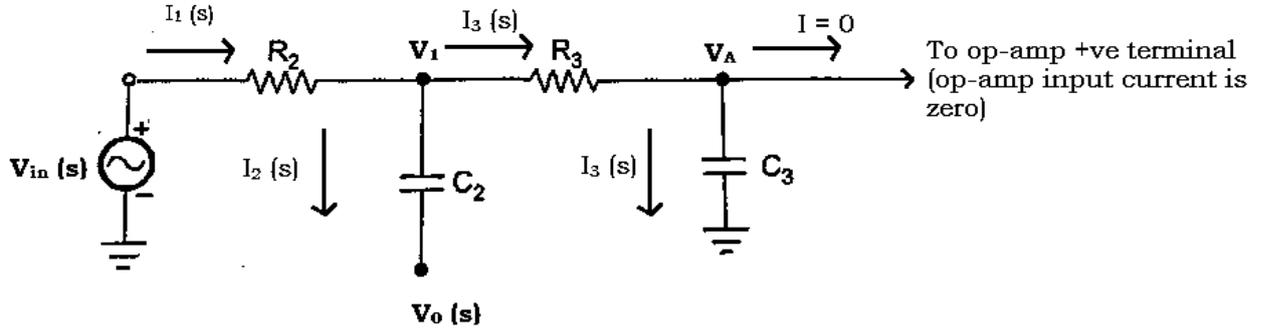
Fig. 3.11 Laplace domain of RC Network

$\rightarrow$ Using potential divider rule, we can write,

$$V_A = V_1 \left[\frac{\frac{1}{sC_3}}{R_3 + \frac{1}{sC_3}}\right] \qquad \rightarrow (3)$$

$$V_A = \frac{V_1}{1 + sR_3C_3}$$

$$\therefore \ V_1 = V_A(1 + sR_3C_3) \qquad \rightarrow (4)$$

$\rightarrow$ Substituting in equation (2) and solving for V_A, we get,

$$\frac{V_{in} - V_A(1 + sR_3C_3)}{R_2} = \frac{V_A(1 + sR_3C_3) - V_0}{\left(\frac{1}{sC_2}\right)} + \frac{V_A(1 + sR_3C_3) - V_A}{R_3}$$

$$\frac{V_{in}}{R_2} + V_0(sC_2) = V_A\left[\frac{(1 + sR_3C_3)}{R_2} + sC_2(1 + sR_3C_3) + \frac{(1 + sR_3C_3)}{R_3} - \frac{1}{R_3}\right]$$

$$\therefore \quad \frac{V_{in}}{R_2} + V_0(sC_2) = V_A\left[\frac{R_3(1 + sR_3C_3) + R_2R_3sC_2(1 + sR_3C_3) + R_2(1 + sR_3C_3) - R_2}{R_2R_3}\right]$$

$$\therefore \quad (R_3V_{in} + V_0sR_2R_3C_2) = V_A[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2]$$

$$V_A = \frac{R_3V_{in} + V_0sR_2R_3C_2}{[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2]}) \qquad \rightarrow (5)$$

$\rightarrow$ Now, for op-amp in non-inverting configuration,

$$V_0 = A_F V_A$$

where,

$$A_F = 1 + \frac{R_f}{R_1} \qquad \rightarrow (6)$$

and $\qquad\quad V_A = The\ voltage\ at\ the\ non-inverting\ terminal$

$$V_0 = A_F\left[\frac{R_3V_{in} + V_0sR_2R_3C_2}{[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2]}\right]$$

$$\therefore \quad \frac{A_FR_3V_{in}}{[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2]} = V_0\left[1 - \frac{sR_2R_3C_2}{[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2]}\right]$$

$$\therefore \quad A_FR_3V_{in} = V_0[(1 + sR_3C_3)(R_3 + R_2R_3sC_2 + R_2) - R_2] - sR_2R_3C_2$$

$$\therefore \quad \frac{V_0}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3C_3 + R_2C_3 + R_2C_2 - A_FR_2C_2)s}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_2C_3}} \qquad \rightarrow (7)$$

$\rightarrow$ As the order of s in the gain expression is two, the filter is called **second order filter**.

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→ The standard form of the transfer function of any second order system is,

$$\frac{V_0}{V_{in}} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2} \qquad \rightarrow (8)$$

where, A = Overall gain

ξ = Damping of system

ω_n = Natural frequency of oscillations

→ Comparing equation (7) and (8), we can say that,

$$\omega_n^2 = \frac{1}{R_2 R_3 C_2 C_3} \qquad \rightarrow (9)$$

→ In case of filters, this frequency is nothing but the cut-off frequency, ω_H

∴ $\qquad \omega_H^2 = \dfrac{1}{R_2 R_3 C_2 C_3}$

∴ $\qquad (2\pi f_H)^2 = \dfrac{1}{R_2 R_3 C_2 C_3}$

$$\therefore \qquad f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} \qquad \rightarrow (10)$$

This is the required cut-off frequency.

→ Replacing s by jω, the transfer function can be written in the frequency domain and hence, finally, can be expressed in the polar form as,

$$\frac{V_0}{V_{in}} = \left|\frac{V_0}{V_{in}}\right| < \varphi$$

where,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}} \qquad \rightarrow (11)$$

where, A_F = Gain of filter in pass band

f = Input frequency in Hz

f_H = High cut-off frequency in Hz

→ The frequency response is shown in fig.3.12.
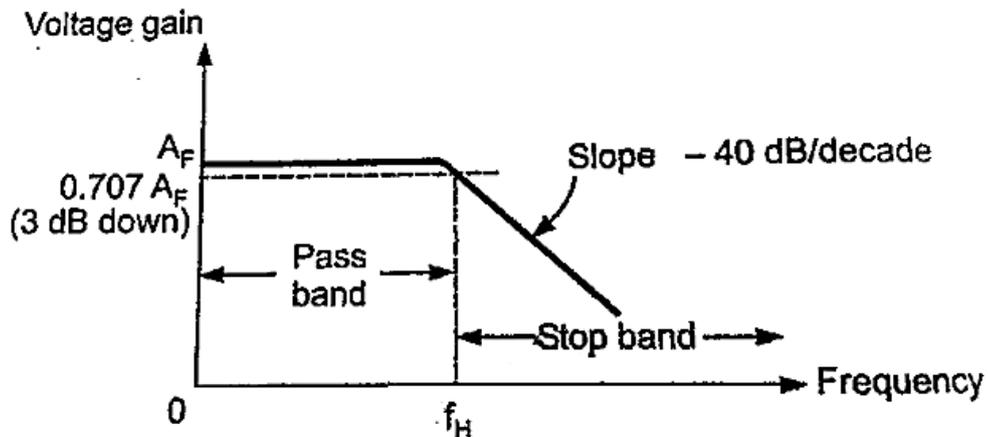
Fig. 3.12 Frequency Response

→ At the cut-off frequency, f_H, the gain is 0.707 A_F i.e. 3 dB down from its 0 Hz level.

→ After, f_H (f >f_H), the gain rolls off at a rate of 40 dB / decade.

→ Hence, the slope of the response after f_H is – 40 dB / decade.

5.2.2 Design steps:

→ The design steps for second order low pass Butterworth filter are:

   ➢ Choose the cut-off frequency f_H.

   ➢ The design can be simplified by selecting $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and choose a value of C less than or equal to 1 µF.

   ➢ Calculate the value of R from the equation,

   ➢ $f_H = \dfrac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \dfrac{1}{2\pi RC}$

   ➢ As $R_2 = R_3 = R$ and $C_2 = C_3 = C$, the pass band voltage gain $A_F = (1 + R_f/R_1)$ of the second order low pass filter has to be equal to 1.586.

→ **Note:** For $R_2 = R_3 = R$ and $C_2 = C_3 = C$, the transfer function takes the form,

$$\frac{V_0(s)}{V_{in}(s)} = \frac{A_F}{s^2 + \dfrac{3 - A_F}{RC}s + \dfrac{1}{R^2 C^2}} \qquad \rightarrow (12)$$

→ From this we can write that,

$$\xi = \text{Damping factor} = (3 - A_F)/2 \quad \rightarrow (13)$$

→ Now, for second order Butterworth filter, the middle term required is $\sqrt{2} = 1.414$, from the normalised Butterworth polynomial.

$$\therefore \qquad 3 - A_F = \sqrt{2} = 1.414$$

$$\therefore \qquad A_F = 1.5862 \qquad\qquad\qquad \rightarrow (14)$$

→ Thus, to ensure the Butterworth response, it is necessary that the gain A_F is 1.586.

$$\therefore \qquad 1.586 = 1 + \frac{R_f}{R_1}$$

$$\therefore \qquad R_f = 0.586 R_1 \qquad\qquad\qquad \rightarrow (15)$$

→ Hence, choose a value of $R_1 \leq 100 \text{ k}\Omega$ and calculate the corresponding value of R_f.

5.3 FIRST ORDER HIGH PASS BUTTERWORTH FILTER:

8. Discuss the second order high pass filter with its frequency response.

→ A high pass filter is a circuit that attenuates all the signals below a specified cut-off frequency denoted as f_L.

→ Thus, a high pass filter performs the opposite function to that of a low pass filter.

→ Hence, the high pass filter circuit can be obtained by interchanging the frequency determining resistances and capacitors in low pass filter circuit.

→ The first order high pass filter can be obtained by interchanging the elements R and C in the first order low pass filter circuit as shown in Fig. 3.13.

→ The frequency at which the gain is 0.707 times the gain of filter in pass band is called **low cut-off frequency** and denoted as f_L.

→ So, all the frequencies greater than f_L is allowed to pass but the maximum frequency which is allowed to pass is determined by the closed loop band-width of the op-amp.
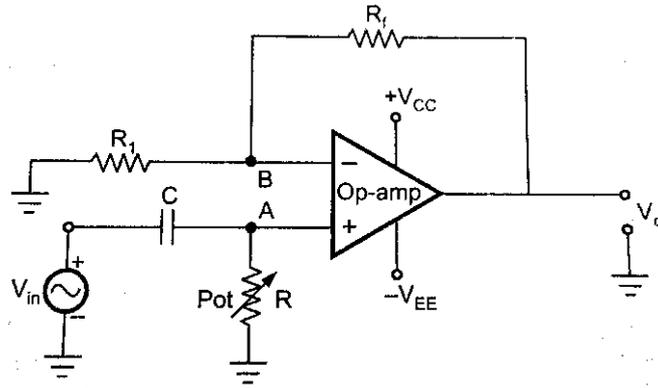
Fig. 3.13 First Order High Pass Butterworth Filter

5.3.1 Analysis of the Filter Circuit:

→ The impedance of the capacitor is, $-jX_C$, where,

$$X_C = \frac{1}{2\pi f C}$$

→ By the potential divider rule, the voltage at the non-inverting input terminal A which is the voltage across capacitor C is given by,

$$V_A = \left[\frac{R}{R - jX_C}\right]V_{in}$$

$$\therefore \quad V_A = \frac{R}{R - j\left(\frac{1}{2\pi f C}\right)} \cdot V_{in} = \frac{2\pi f C}{2\pi f R C - j} \cdot V_{in} = V_{in}\left[\frac{j2\pi f C}{\frac{2\pi f R C}{-j} + 1}\right]$$

but $-j = 1/j$ and $-1/j = j$

$$\therefore \quad V_A = V_{in}\left[\frac{j2\pi f C}{j2\pi f R C + 1}\right]$$

→ This can be represented as,

$$V_A = V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

where,

$$f_L = \frac{1}{2\pi f C} = Low\ cut - off\ frequency$$

→ Now, for the op-amp in the non-inverting configuration,

$$V_0 = A_F V_A$$

where, V_A = voltage at the non-inverting input

and $A_F = \left(1 + \frac{R_f}{R_1}\right)$ = gain of op-amp in pass band

$$\therefore \quad V_0 = A_F V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

i.e.

$$\frac{V_0}{V_{in}} = A_F\left[\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right]$$

→ This is the transfer function of the filter and can be expressed in the polar form as,

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$$\frac{V_0}{V_{in}} = \left|\frac{V_0}{V_{in}}\right| < \varphi$$

where,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

→ The above equation describes the behaviour of the high pass filter.

❖ At very low frequencies, f <f_L

❖ $\left|\frac{V_0}{V_{in}}\right| < A_F$

❖ At f = f_L,

❖ $\left|\frac{V_0}{V_{in}}\right| = 0.707 A_F$ i.e. 3 dB down from the level of A_F

❖ At f >f_L, i.e. high frequencies, 1 can be neglected as compared to (f/f_L) from denominator.

$$\therefore \qquad \left|\frac{V_0}{V_{in}}\right| \cong A_F \ i.e. constant$$

→ Thus the circuit acts as high pass filter with a pass band gain as A_F.

→ For the frequencies f <f_L, the gain increases till f = f_L at a rate of + 20 dB / decade.

→ Hence, the slope of the frequency response in stop band is + 20 dB / decade for first order high pass filter.

→ The frequency response is shown in the Fig.3.14.
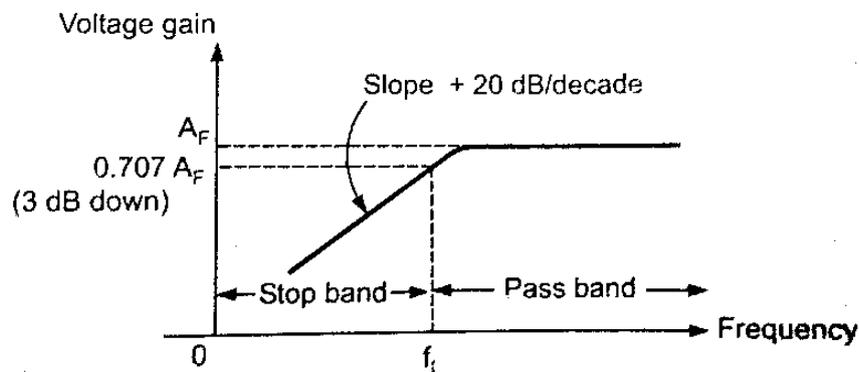
Fig. 3.14 Frequency Response

5.3.2 Design steps:

→ The design steps for the first order high pass Butterworth filter are,

❖ Choose the cut-off frequency, f_L.

❖ Choose the capacitance C usually between 0.001 and 1µF. Generally, it is selected as 1µF or less than that. For better performance, Mylar or Tantalum capacitors are selected.

❖ Now, for the RC circuit,

$$f_L = \frac{1}{2\pi f C}$$

Hence, as f_H and C are known, calculate the value of R.

❖ The resistance R_f and R_1 can be selected depending on the required gain in the pass band. $\qquad A_F = \left(1 + \frac{R_f}{R_1}\right)$

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5.4 SECOND ORDER HIGH PASS BUTTERWORTH FILTER:

9. Discuss the second order high pass filter with its frequency response and design the circuit with cut-off frequency of 5 KHZ. (May-15) (8)

→ The second order high pass Butterworth produces a gain roll off at the rate of + 40 dB / decade in the stop band.

→ This filter can also be realised by interchanging the positions of resistors and capacitors in a second order low pass Butterworth filter.

→ The Fig. 3.15 shows the second order high pass Butterworth filter.
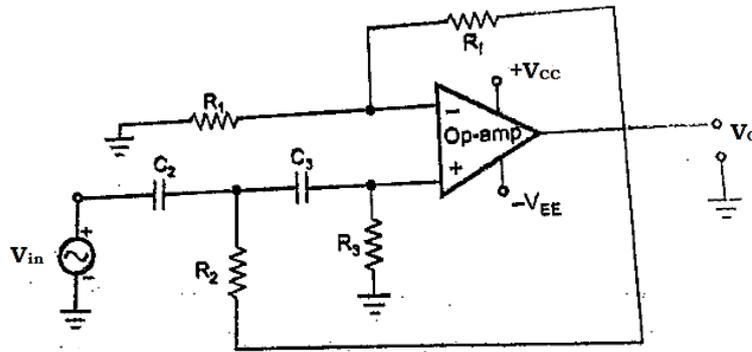
Fig. 3.15 Second Order High Pass Butterworth Filter

→ The analysis, design and the scaling produces for this filter is exactly the same as that of second order low pass Butterworth filter.

→ The voltage magnitude equation for the second order high pass filter is,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

where, f = input frequency in Hz

$$f_L = lower\ cut-off\ frequency\ in\ Hz = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

→ For, $R_2 = R_3 = R$ and $C_2 = C_3 = C$,

$f_L = 1/2\pi RC$

A_F=Pass band gain=1.586 to ensure second order Butterworth response

and $R_f = 0.586\ R_1$

→ The frequency response of this filter is shown in the Fig.3.16.
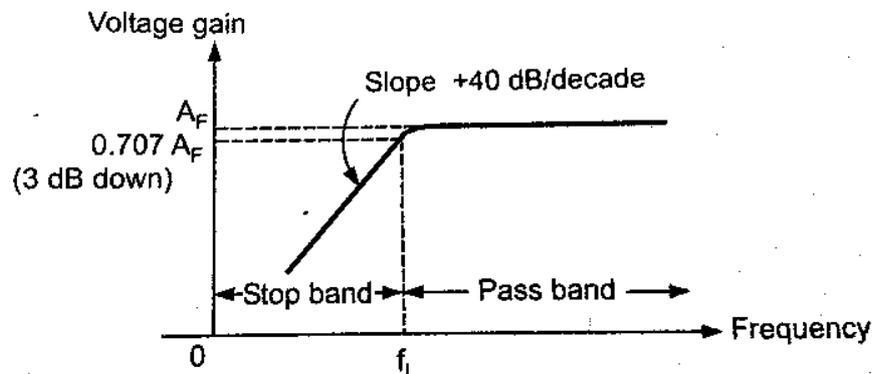
Fig. 3.16 Frequency Response

10. Explain in detail of comparator circuit.

6.1 COMPARATOR:

→ A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.

→ It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig.3.17 (a).

→ However, a commercial op-amp has the transfer characteristics of Fig. 17 (b).
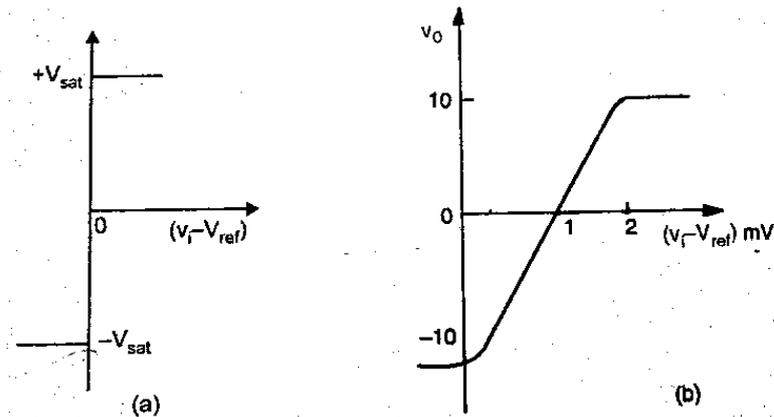
Fig. 3.17 Transfer Characteristics (a) Ideal Comparator (b) Practical Comparator

→ It may be seen that the change in the output state takes place with an increment in input V_i of only 2 mV.

→ This is the uncertainty region where output cannot be directly defined.

→ There are basically two types of comparators:
  - ➢ Non-inverting comparator
  - ➢ Inverting comparator

→ The circuit of Fig.3.18 is called a non-inverting comparator.
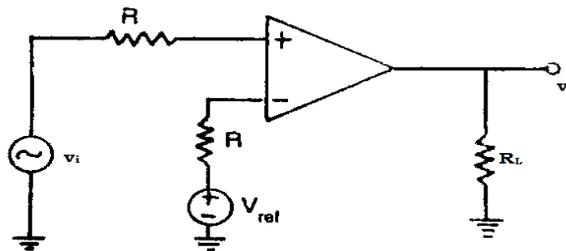
Fig. 3.18 Non-inverting comparator

→ A fixed reference voltage V_{ref} is applied to (−) input and a time varying signal V_i, is applied to (+) input. The output voltage is at $-V_{sat}$, for $V_i < V_{ref}$ and V_0 goes to $+ V_{sat}$ for $V_i > V_{ref}$.

→ The output waveforms for a sinusoidal input signal applied to the (+) input is shown in Fig.3.19for positive and negative V_{ref} respectively.
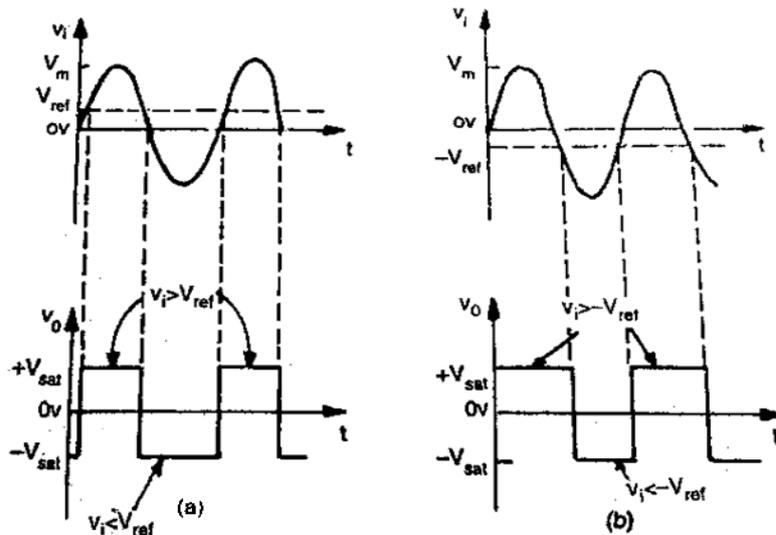
Fig. 3.19 Input and output waveforms for (a) V$_{ref}$ positive (b) V$_{ref}$ negative

→ In a practical circuit V$_{ref}$ is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages V+ and V–with the wiper connected to (–) input terminal as shown in Fig.3.20.
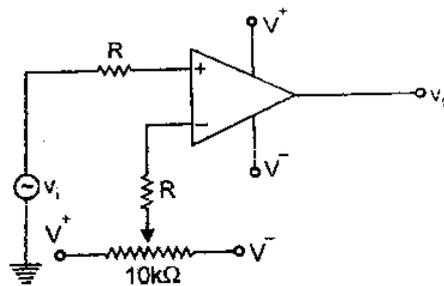
Fig. 3.20 Practical Non-inverting comparator

→ Thus a V$_{ref}$of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

→ Fig.3.21 shows a practical inverting comparator in which the reference voltage V$_{ref}$ is applied to the (+) input and V$_i$, is applied to (–) input.
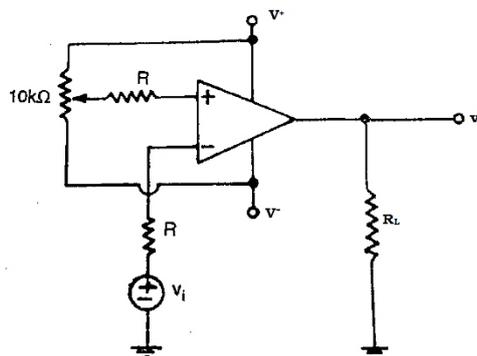
Fig. 3.21 Inverting Comparator

→ For a sinusoidal input signal, the output waveform is shown in Fig.3.22 for V$_{ref}$ positive and negative respectively.
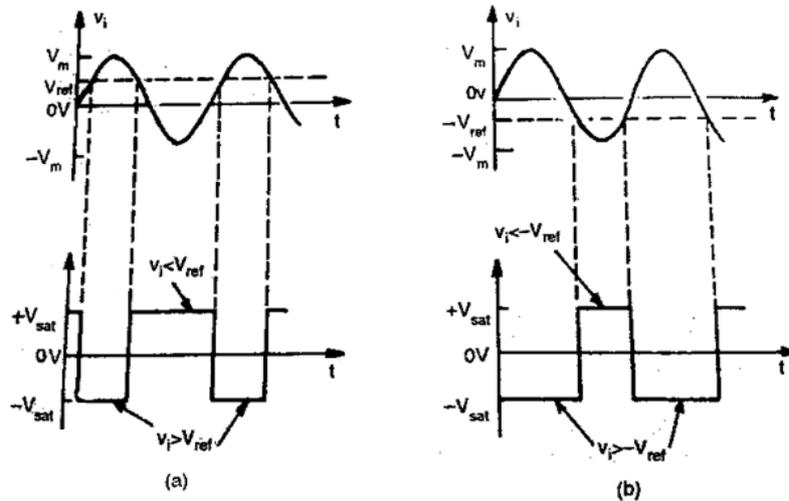
Fig. 3.22 Input and output waveforms for (a) V_{ref} positive (b) V_{ref} negative

→ Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig.3.23.
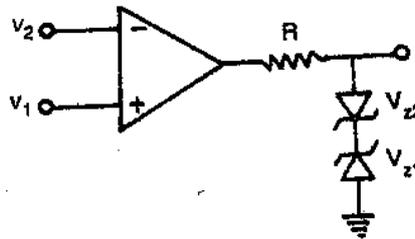
Fig. 3.23 Comparator with zener diode at the output

→ The value of resistance R is chosen so the zener diode operates at the recommended current.

→ It can be seen that the limiting voltages of V_0 are $(V_{z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~ 0.7 V) is the diode forward voltage.

→ In the waveforms of Fig.3.19 and 3.22, the output transitions are shown as taking place instantaneously.

→ Practical circuits, however, take a certain amount of time to switch from one voltage level to another.

→ The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing.

→ These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself.

→ Thus there is an upper limit to the operating frequency of any comparator.

6.2 Applications of Comparator:

→ Some important applications of comparator are:
- ❖ Zero crossing detector
- ❖ Window detector
- ❖ Time marker generator
- ❖ Phase meter

6.2.1 Zero Crossing Detector:

→ The basic comparators of Fig.3.18 and 3.21 can be used as a zero crossing detector provided that V_{ref} is set to zero.

$\rightarrow$ An inverting zero-crossing detector is shown in Fig. 24 (a) and the output waveform for a Sinusoidal input signal is shown in Fig. 24 (b)
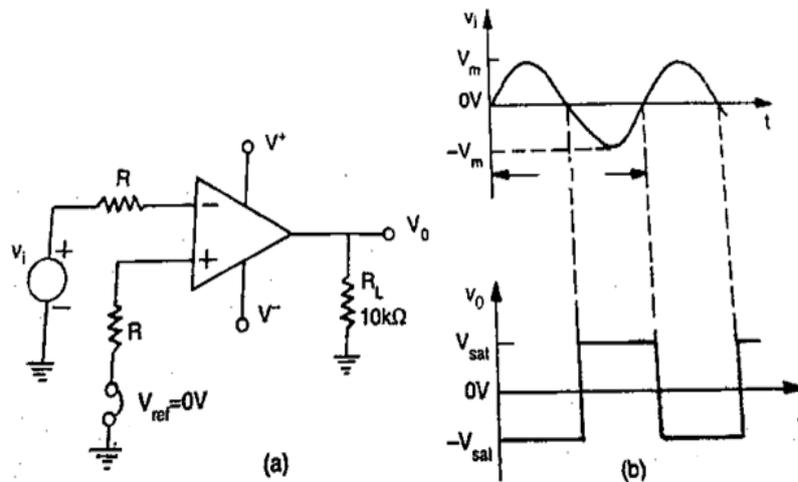
Fig. 3.24 (a) Zero crossing detector (b) Input and Output Waveforms

$\rightarrow$ The circuit is also called a sine to square wave generator.

6.2.2 Window Detector:

$\rightarrow$ Sometimes one may like to mark the instant at which an unknown input is between two threshold levels.

$\rightarrow$ This can be achieved by a circuit called window detector.

$\rightarrow$ Fig. 3.25 shows a three level detector with indicator circuit.
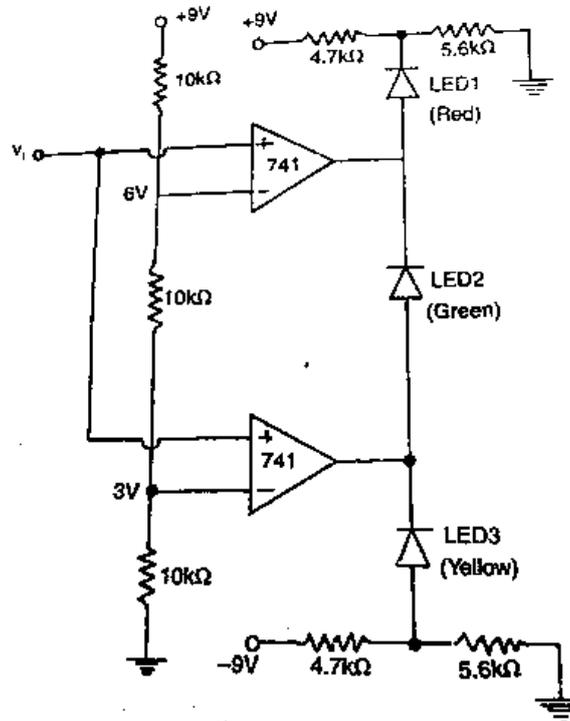
Fig. 3.25 Three level comparator with LED indicator

$\rightarrow$ There are three indicators: Yellow (LED 3) for input too low (<3V), Green (LED 2) for safe input (3 – 6V) and Red (LED 1) for high input (> 6V). They are turned on and off as indicated in Table 3.1.

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Table 3.1 Three level comparator specifications

Input (V)	Yellow LED 3	Green LED 2	Red LED 1
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6 V	Off	Off	On

6.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

11. Explain the operation of Schmitt trigger. (Dec – 14)
(or)
With the neat circuit diagram explain the working of Schmitt trigger using op-amp. (May-15) (8)

→ If positive feedback is added to the comparator circuit, gain can be increased greatly.

→ Consequently, the transfer curve of comparator becomes more close to ideal curve.

→ Theoretically, if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes infinite.

→ This results in an abrupt (zero rise time) transition between the extreme values of output voltage.

→ In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations.

→ So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage.

→ This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

→ Fig. 3.26 shows such a regenerative comparator. The circuit is also known as Schmitt Trigger.
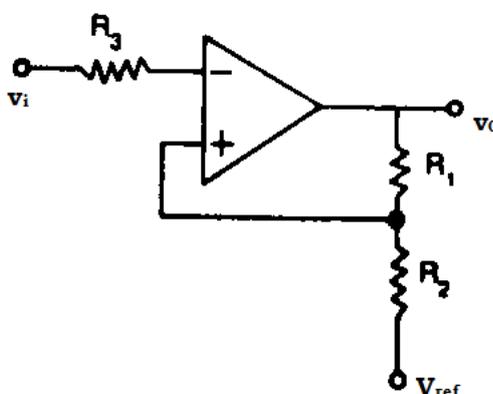
Fig. 3.26 An inverting Schmitt trigger

→ The input voltage is applied to the (–) input terminal and feedback voltage to the (+) input terminal.

→ The input voltage V_i triggers the output V_0 every time it exceeds certain voltage levels.

→ These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}).

→ The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$.

→ These threshold voltages are calculated as follows.

→ Suppose the output $V_0 = + V_{sat}$, then the voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 - R_2}\left(V_{sat} - V_{ref}\right) = V_{UT}$$

→ This voltage is called upper threshold voltage V_{UT}.

→ As long as V_i is less than V_{UT}, the output V_0 remains constant at $+V_{sat}$.

→ When V_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $V_i > V_{UT}$ as shown in Fig.3.27 (a).

→ For $V_0 = -V_{sat}$, the voltage at the (+) input terminal is

$$V_{ref} - \frac{R_2}{R_1 - R_2}\left(V_{sat} + V_{ref}\right) = V_{LT}$$

→ This voltage is referred to as lower threshold voltage V_{LT}.

→ The input voltage V_i must become lesser than V_{LT} in order to cause V_0 to switch from $-V_{sat}$ to $+V_{sat}$.

→ A regenerative transition takes place as shown in Fig.3.27 (b) and the output V_0 returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously.

→ The complete transfer characteristics are shown in Fig.3.27 (c).
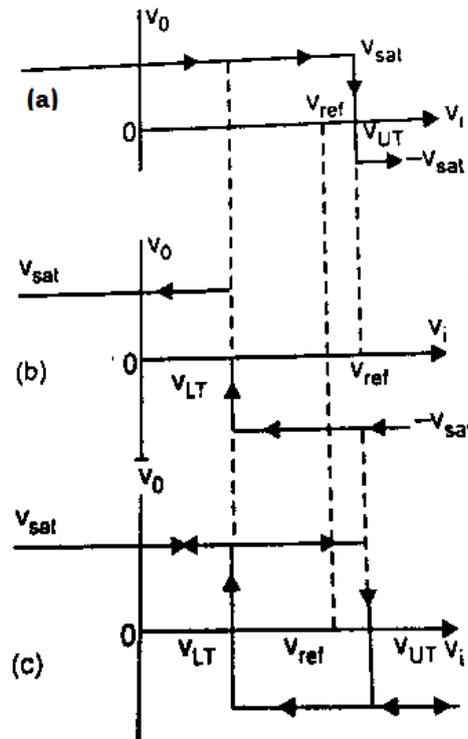
Fig. 3.27 (a, b) Transfer characteristics for v_i increasing and v_i decreasing
(c) Composite input-output curve

→ Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2}$$

→ Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones.

→ Further, note that if peak-to-peak input signal V_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return to $-V_{sat}$.

→ It may be seen from the equation of V_H that hysteresis width V_H is independent of V_{ref}.

→ The resistor R_3 in Fig. 3.26 is chosen equal to $R_1 \parallel R_2$ to compensate for the input bias current.

→ A non-inverting Schmitt trigger is obtained if V_i and V_{ref} are interchanged in Fig.3.26.

→ The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig.3.28.
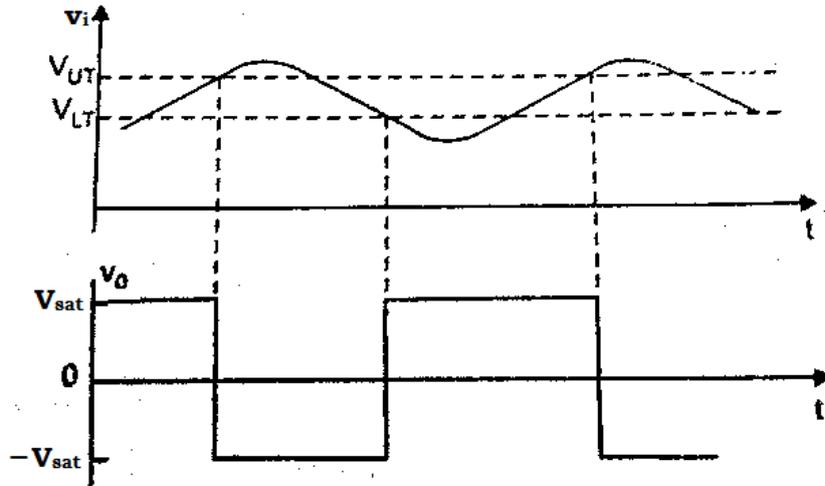
Fig. 3.28 Schmitt trigger used as a squarer

→ If in the circuit of Fig. 3.26, V_{ref} is chosen as zero volt, so we can write,

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

→ If an input sinusoid of frequency f = 1/T is applied to such a comparator, a symmetrical square wave is obtained at the output.

→ The vertical edge of the output waveform however will not occur at the time the sine wave passes through zero but is shifted in phase by θ where sin θ = V_{UT}/V_m and V_m is the peak sinusoidal voltage as shown in Fig. 3.29.
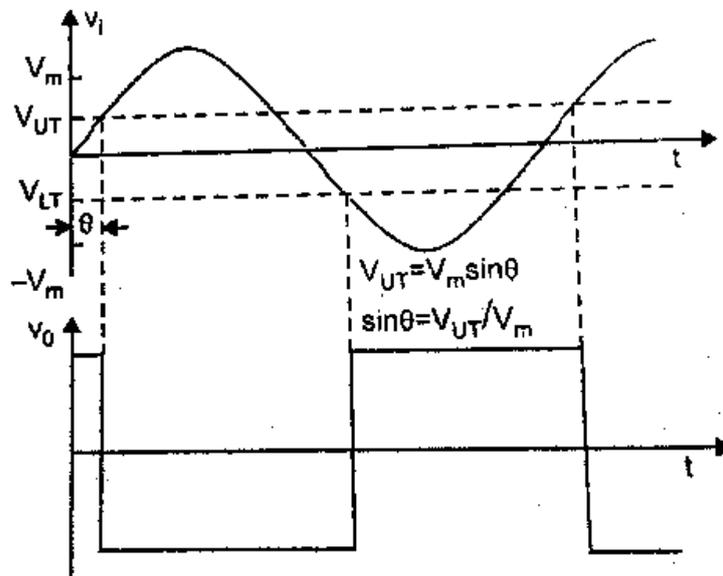
Fig. 3.29 Shift θ in the output waveform for $V_{UT} = - V_{LT}$

7. MULTIVIBRATORS

7.1 ASTABLE MULTIVIBRATOR: (SQUARE WAVE GENERATOR)

12. Draw the circuits of Astable multivibrator and obtain expression for pulse width T.

→ A simple op-amp square wave generator is shown in Fig. 3.30.

→ Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region.

→ In Fig.3.30 fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal.
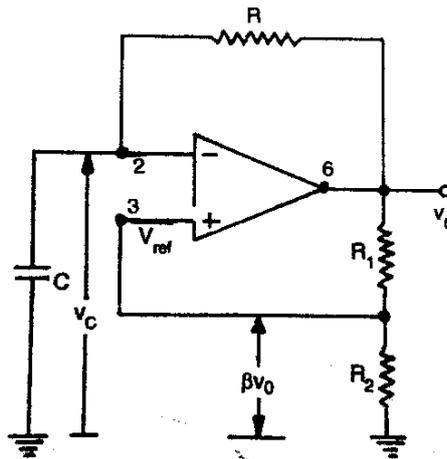
Fig. 3.30 Simple op-amp square wave generator

→ Thus the reference voltage V_{ref} is βV_0 and may take values as $+ \beta V_{sat}$ or $- \beta V_{sat}$.

→ The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination.

→ Whenever input at the (–) input terminal just exceeds V_{ref}, switching takes place resulting in a square wave output.

→ In an astable multivibrator, both the states are quasi stable.

→ Consider an instant of time when the output is at $+V_m$.

→ The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig.3.31.
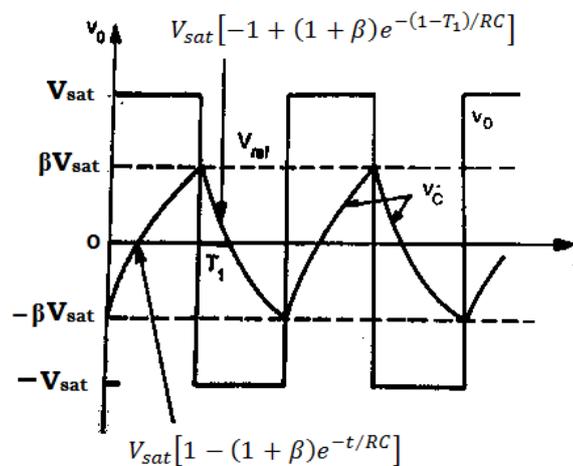
Fig. 3.31 Waveforms

→ The voltage at the (+) input terminal is held at $+ \beta V_{sat}$ by R_1 and R_2 combination.

→ This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage.

→ When the voltage at the $(-)$ input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$.

→ It begins to discharge through R, that is, charges toward $-V_{sat}$.

→ When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$.

→ The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 31.

→ The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa.

→ The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}(1 + \beta)e^{-t/RC}$$

→ At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place. Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1 + \beta)e^{-t/RC}$$

→ After algebraic manipulation, we get,

$$T_1 = RC \ln\frac{1 + \beta}{1 - \beta}$$

→ This gives only one half of the period.

→ Total time period is given as,

$$T = 2T_1 = 2RC \ln\frac{1 + \beta}{1 - \beta}$$

as the output waveform is symmetrical.

→ If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that,

$$T = 2RC$$

or

$$f_0 = \frac{1}{2RC}$$

→ The output swings from $+V_{sat}$ to $-V_{sat}$, so,

$$V_0 \text{ (peak-to-peak)} = 2V_{sat}$$

→ The peak to peak output amplitude can be varied by varying the power supply voltage.

→ However, a better technique is to use back to back zener diodes as shown in Fig. 32.

→ The output voltage is regulated to $\pm(V_Z + V_D)$ by the zener diodes.

$$V_0 \text{ (peak-to-peak)} = 2(V_Z + V_D)$$

→ Resistor R_{SC} limits the currents drawn from the op-amp to,

$$I_{SC} = \frac{V_{sat} - V_Z}{R_{SC}}$$

→ This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.
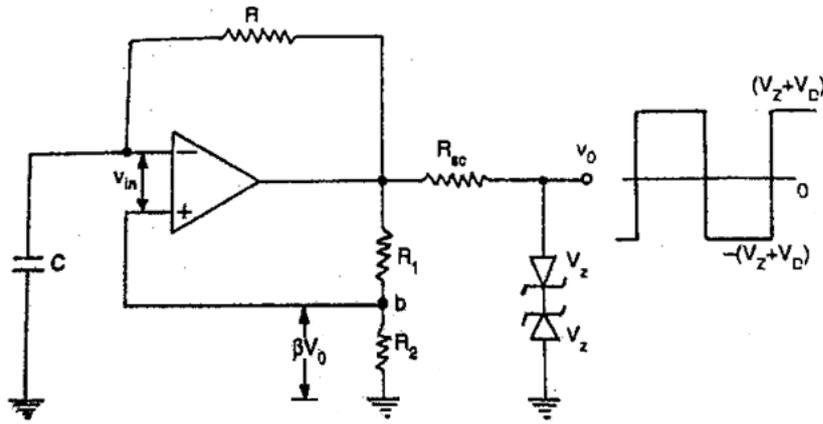
37

Fig. 3.32 Use of back to back zener diodes

→ If an asymmetric square wave is desired, then zener diodes with different break down voltages V_{Z1} and V_{Z2} may be used.

→ Then the output is either V_{01} or V_{02}, where $V_{01} = V_{Z1} + V_D$ and $V_{02} = V_{Z2} + V_D$.

→ It can be easily shown that the positive section is given by,

$$T_1 = RC \, ln \frac{1 + \beta \, V_{01}/V_{02}}{1 - \beta}$$

→ The duration of negative section T_2 will be the same as T_1 with V_{01} and V_{02} interchanged.

→ An alternative method to get asymmetric square wave output is to add a d.c. voltage source V in series R_2 as shown in Fig.3.33.
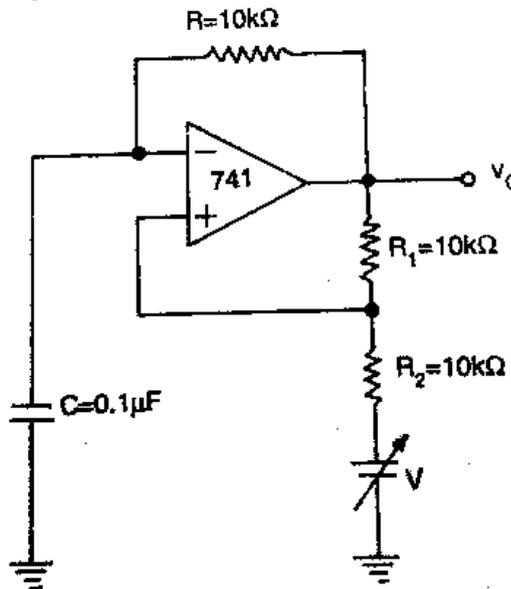
Fig. 3.33 Asymmetric Square Wave Generator

→ Now the capacitor C swings between the voltage levels ($\beta V_{sat} + V$) and ($-\beta V_{sat} + V$).

→ If the voltage source V is made variable, voltage to frequency conversion can be achieved, though the variation will not be linear.

7.2. MONOSTABLE MULTIVIBRATOR:

13. Draw the circuits of Mono stable multivibrator and obtain expression for pulse width T.

→ Mono stable multivibrator has one stable state and the other is quasi stable state.

→ The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.

$\rightarrow$ The width of the output pulse depends only on external components connected to the op-amp.

$\rightarrow$ The circuit shown in Fig. 3.34 is a modified form of an astable multivibrator.
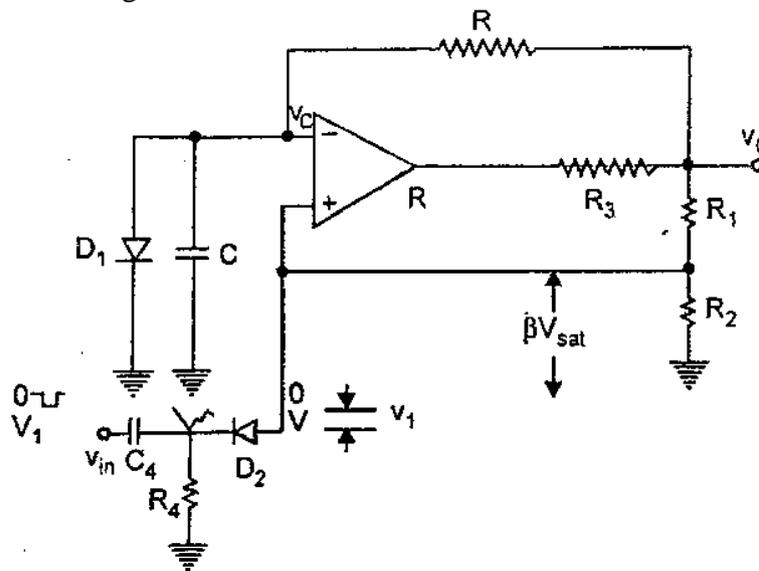
Fig. 3.34 Mono stable multivibrator

$\rightarrow$ A diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+ V_{sat}$.

$\rightarrow$ A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

$\rightarrow$ To analyse the circuit, let us assume that in the stable state, the output V_0 is at $+ V_{sat}$.

$\rightarrow$ The diode D_1 conducts and v_C the voltage across the capacitor C gets clamped to $+ 0.7V$.

$\rightarrow$ The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+ \beta V_{sat}$.

$\rightarrow$ Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V i.e. ($[\beta V_{sat} + (-V_1)] < 0.7$ V), the output of the op-amp will switch from $+ V_{sat}$ to $-V_{sat}$.

$\rightarrow$ The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R.

$\rightarrow$ The voltage at the (+) input terminal Is now $- \beta V_{sat}$.

$\rightarrow$ When the capacitor voltage v_C becomes just slightly more negative than $- \beta V_{sat}$, the output of the op-amp switches back to $+ V_{sat}$.

$\rightarrow$ The capacitor C now starts charging to $+ V_{sat}$ through R until v_C is 0.7V as capacitor C gets clamped to the voltage.

$\rightarrow$ Various waveforms are shown in Fig.3.35 (a, b, c)
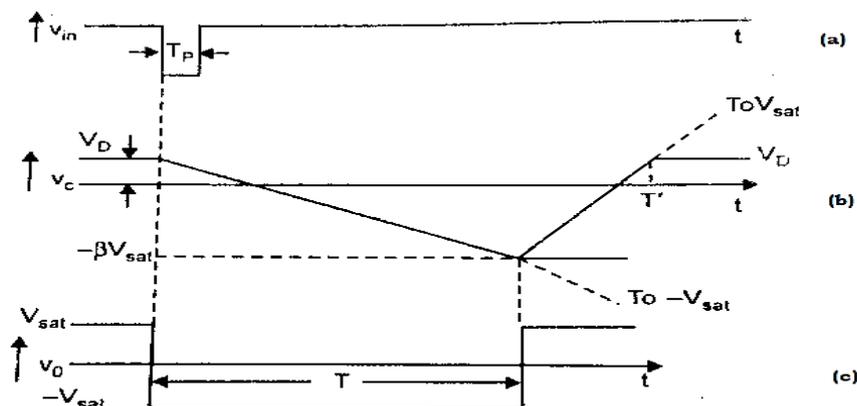
Fig. 3.35 (a) Negative going Trigger Signal (b) Capacitor Waveform
(c) Output Voltage Waveform

→ The pulse width T of mono stable multivibrator is calculated as follows:

→ The general solution for a single time constant low pass RC circuit with V_i, and V_f as initial and final values is,

$$V_0 = V_f + (V_i - V_f)e^{-t/RC}$$

→ For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

→ The output v_C is,

$$v_C = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

At t = T,

$$v_C = -\beta V_{sat}$$

Therefore,

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

→ After simplification, pulse width T is obtained as,

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta}$$

where, $\beta = R_2/(R_1+R_2)$

→ If, $V_{sat} \gg V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then,

$$T = 0.69 RC$$

→ For a mono stable operation, the trigger pulse width T_p should be much less than T, the pulse width of the mono stable multivibrator.

→ The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

→ It may be noted from Fig.3.35 (a) that capacitor voltage v_C reaches its quiescent value V_D at T' > T.

→ Therefore, it is essential that a recovery time T'–T be allowed to elapse before the next triggering signal is applied.

→ The circuit of Fig. 3.34 can be modified to achieve voltage to time delay conversion as in the case of square wave generator.

→ The mono stable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger.

→ It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

8. WAVEFORM GENERATORS

8.1. SQUARE WAVE GENERATOR:

→ Same as an Astable Multivibrator. Also Schmitt Trigger.

8.2. TRIANGULAR WAVE GENERATOR:

14. With diagram explain the following op- amp applications of triangular wave generation. (May-17, 18) (13)

→ A triangular wave can be simply obtained by integrating a square wave as shown in Fig.3.36.
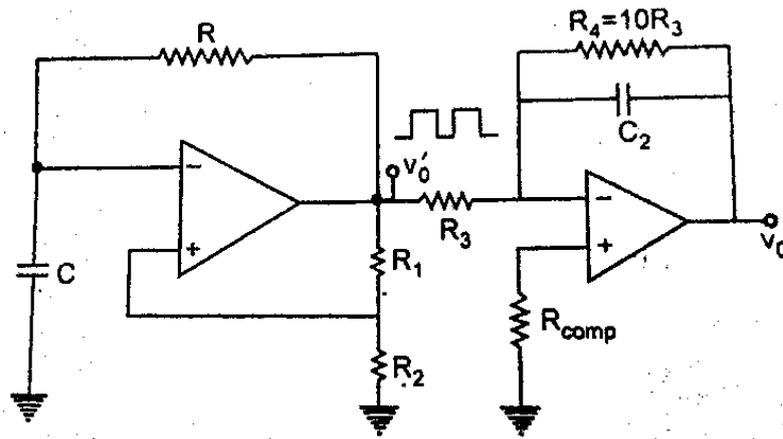
Fig. 3.36 Triangular Waveform Generator

→ It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig.3.37.
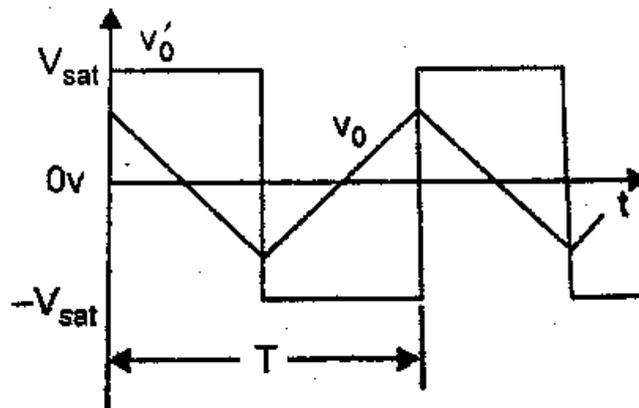

Fig. 3.37 Output Waveform

→ Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases.

→ This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies.

→ A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

→ Another triangular wave generator using lesser number of components is shown in Fig.3.38.
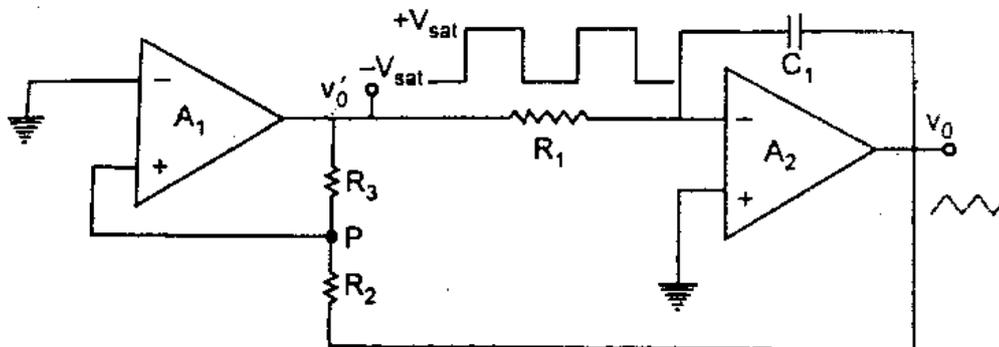
Fig. 3.38 Triangular Wave Generator Using Lesser Components

→ It basically consists of a two level comparator followed by an integrator.

→ The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave.

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→ This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.

→ Initially, let us consider that the output of comparator A_1 is at $+ V_{sat}$.

→ The output of the integrator A_2 will be a negative going ramp as shown in Fig.3.39.
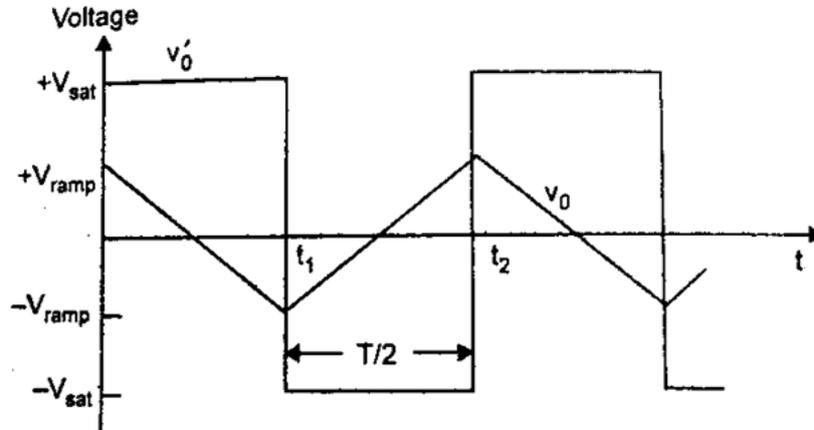
Fig. 3.39 Output Waveforms

→ Thus one end of the voltage divider R_2R_3 is at a voltage $+ V_{sat}$ and the other at the negative going ramp of A_2.

→ At a time $t = t_1$, when the negative going ramp attains a value of $- V_{ramp}$, the effective voltage at point P becomes slightly less than 0V.

→ This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$.

→ During the time when the output of A1 is at $- V_{sat}$, the output of A_2 increases in the positive direction.

→ And at the instant $t = t_2$, the voltage at point P becomes just above 0V, thereby switching the output of A_1 from $-V_{sat}$ to $+ V_{sat}$.

→ The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same.

→ However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2, and the output voltage level of A_1.

→ The output voltage of A_1 can be set to desired level by using appropriate zener diodes.

→ The frequency of the triangular waveform can be calculated as follows:

→ The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - \left(-V_{ramp}\right)\right]$$

→ At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from the above equation,

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat})$$

→ Similarly, at $t = t_2$, when the output of A_1 switches from $- V_{sat}$ to $+ V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat})$$

$$V_{ramp} = \frac{R_2}{R_3}(V_{sat})$$

→ Therefore, peak to peak amplitude of the triangular wave is,

$$v_0(pp) = +V_{ramp} - \left(-V_{ramp}\right)$$

$$v_0(pp) = 2\frac{R_2}{R_3}V_{sat}$$

→ The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integration equation, $(v_0 = -\frac{1}{RC}\int v_i\, dt)$

$$v_0(pp) = -\frac{1}{R_1 C_1}\int_0^{T/2} -V_{sat}\, dt$$

$$v_0(pp) = \frac{V_{sat}}{R_1 C_1}\left(\frac{T}{2}\right)$$

or

$$T = 2R_1 C_1 \frac{v_0(pp)}{V_{sat}}$$

→ Putting the value of $v_0(pp)$ in the above equation,

$$T = \frac{4R_1 C_1 R_2}{R_3}$$

→ Hence the frequency of oscillation f_0 is,

$$f_0 = \frac{1}{T} = \frac{R_3}{4R_1 C_1 R_2}$$

8.3. SINE WAVE GENERATOR:

15. With diagram explain the following op- amp applications of sine wave generation. (Dec – 12) (16)

→ As oscillator is basically a feedback circuit where a fraction v_f of the output voltage v_0 of an amplifier is fed back to the input in the same phase.

→ The block diagram of an oscillator is shown in Fig.3.40.
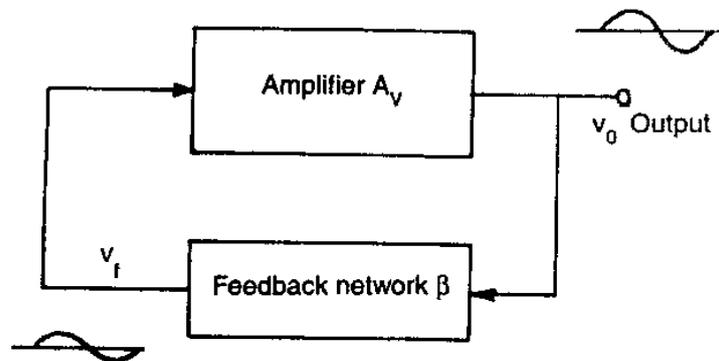
Fig. 3.40 Block diagram of a feedback oscillator

→ For sustained oscillation, $A_V\beta = 1$.

→ That is, magnitude condition $\left|A_V\beta\right| = 1$ and the phase condition, angle $A_V\beta = 0°$ or $360°$ must be simultaneously satisfied in the circuit.

→ There are different types of sine-wave oscillators available according to the range of frequency, namely RC oscillators for audio frequency and LC oscillators for radio frequency range.

→ Here we will discuss only two types of audio frequency RC oscillators.

16. Explain the working principle of RC phase shift sine wave generator using OPAMP and derive the expression for 'f'. (Dec – 14) (16)

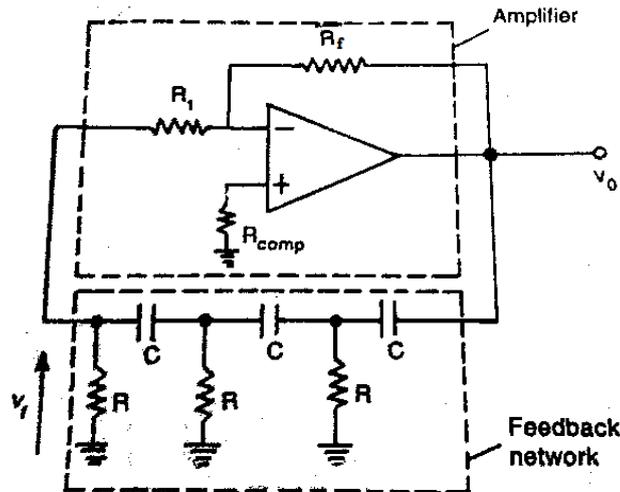**8.3.1 Phase Shift Oscillator:**

Fig. 3.41 Phase Shift Oscillator

→ Figure shows a phase shift oscillator. The op-amp provides a phase shift of 180° as it is used in the inverting mode.

→ An additional phase shift of 180° is provided by the feedback RC network.

→ The transfer function of the RC network can be easily calculated as,

$$\beta = \frac{v_f}{v_0} = \frac{1}{1 + 6/sRC + 5/s^2R^2C^2 + 1/s^3R^2C^3}$$

Let s = jω,

$$\beta = \frac{1}{1 - 5(f_1/f)^2 - j[6(f_1/f) - (f_1/f)^3]}$$

where, $f_1 = \frac{1}{2\pi RC}$

→ For $A_V\beta = 1$, β should be real. So the imaginary term must be equal to zero, that is,

$$6(f_1/f) - (f_1/f)^3 = 0$$
$$\text{or}$$
$$f_1/f = \sqrt{6}$$

→ The frequency of the oscillation f_0 is given by,

$$f_0 = \frac{1}{\sqrt{6}(2\pi RC)}$$

Also, the loop gain $A_V\beta = 1$
$$\text{or}$$
$$\frac{A_V}{1 - 5(f_1/f_0)^2} = 1$$
$$\text{or}$$
$$A_V \geq -29$$

→ That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\,R_1$.

→ The gain A_V is kept greater than 29 to ensure that variations in circuit parameters will not make $|A_V\beta| < 1$, otherwise oscillations will die out.

→ For low frequencies (<1 kHz), op-amp 741 may be used, however for high frequencies, LM 318 or LF 351 should be used.

8.3.2 Wien Bridge Oscillator:

→ Another commonly used audio frequency oscillator is a Wien bridge oscillator.

→ The circuit is shown in Fig.3.42.It may be noted that the feedback signal in this circuit is connected to the (+) input terminal so that the op-amp is working as a non-inverting amplifier.
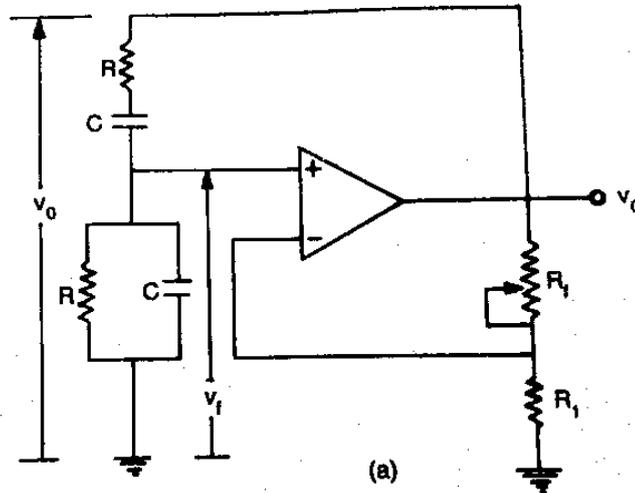

Fig. 3.42 Wien Bridge Oscillator

→ Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series RC network in one arm and a parallel RC network in the adjoining arm.

→ Resistors R_1 and R_f are connected in the remaining two arms. The condition of zero phase shifts around the circuit is achieved by balancing the bridge.

→ From the feedback network, the feedback factor β is,

$$\beta = \frac{v_f}{v_0} = \frac{R/(1 + j\omega RC)}{[(R - j/\omega C) + R/(1 + j\omega RC)]}$$

$$\beta = \frac{R}{3R + j(\omega R^2 C - 1/\omega C)}$$

For $A_V\beta = 1$, β must be real. That is the imaginary part is zero.

$$\therefore \ \omega R^2 C - \frac{1}{\omega C} = 0$$

or

$$\omega = \frac{1}{RC}$$

The frequency of oscillation f_0 is,

$$f_0 = \frac{1}{2\pi RC}$$

→ At f_0,β is equal to 1/3. Therefore, for sustained oscillation, the amplifier must have a gain of precisely 3.

→ However, from practical point of view, A_V may be slightly less or greater than 3.

→ For A_V< 3, the oscillations will either die down or fail to start when power is first applied.

→ And, for A_V> 3, the oscillations will be growing. This problem is eliminated by a practical Wien bridge oscillator with adaptive negative feedback as shown in Fig.3.43.
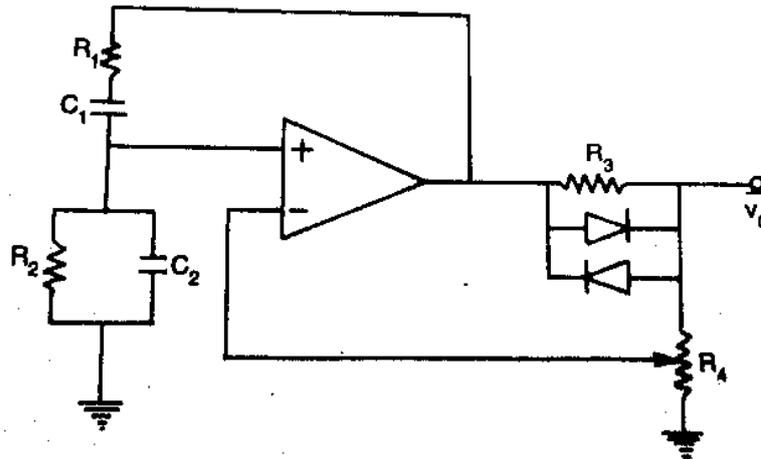
Fig. 3.43 Practical Wien Bridge Oscillator with adaptive negative feedback

→ In this circuit, resistor R_4 is initially adjusted to give a gain so that oscillations start.

→ The output signal grows in amplitude until the voltage across R_3 approaches the cut-in voltage of the diode.

→ As the diodes begin to turn-on (one for the positive half cycle and the other for the negative half cycle), the effective feedback resistance R_f decreases because the diode is in parallel with the resistance R_3.

→ This will reduce the gain of the amplifier which in turn lowers the output amplitude.

→ Hence sustained oscillations can be obtained. Further, if the output signal falls, the diodes would begin to turnoff thereby increasing R_f which in turn increases gain.

9. CLIPPERS

17. Draw a circuit of a clipper which will clip the input signal below the reference voltage. (Dec – 14, 15) (May – 17) (8)

(or)

Elaborate with neat circuit diagram, and input/ output waveforms, the operation of positive clipper. (Nov/Dec 2019) (6)

→ A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

→ Fig. 44 shows a positive clipper. The clipping level is determined by the reference voltage V_{ref} and could be obtained from the positive supply voltage V^+.
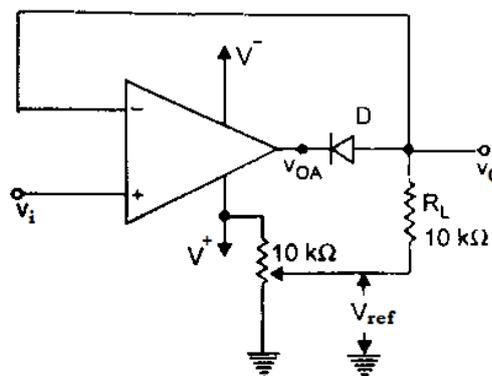
Fig. 3.44 Positive Clipper Circuit

→ The input and output waveforms are, shown in Fig. 3.45 (a). It can be seen that the portion of the output voltage for $v_0 > V_{ref}$ are clipped off.
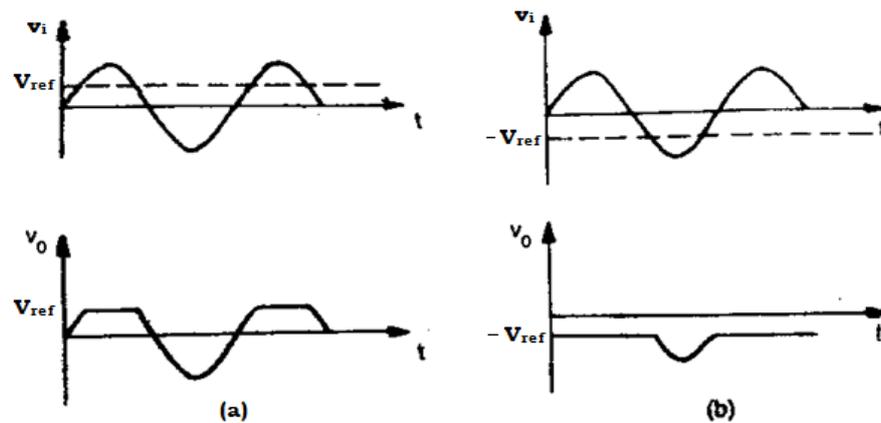

Fig. 3.45 Input and output Waveforms for (a) positive V_{ref} (b) Negative V_{ref}

→ For input voltage $v_i < V_{ref}$, diode D conducts. The op-amp works as a voltage follower and output v_0 follows input v_i till $v_i \leq V_{ref}$. When v_i is greater than V_{ref}, the output v_{0A} of the op-amp is large enough to drive D into cut-off.

→ The op-amp operates in the open-loop and output voltage $v_0 = V_{ref}$.

→ However, if V_{ref} is made negative, then the entire output waveform above V_{ref} will get clipped off as shown in fig.3.45 (b).

→ The positive clipper of Fig. 44 can be easily converted into a negative clipper by reversing diode D and changing the polarity of the V_{ref}, as shown in Fig. 3.46.
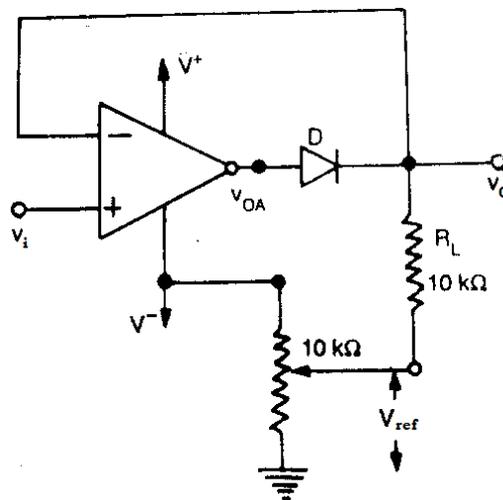
Fig. 3.46 Negative Clipper Circuit

→ The negative clipper clips off the negative parts of the input signal below the reference voltage.

→ The circuit diagram of a negative clipper and the expected waveforms for negative V_{ref}, and positive V_{ref}, are shown in Fig.3.47 (a, b).
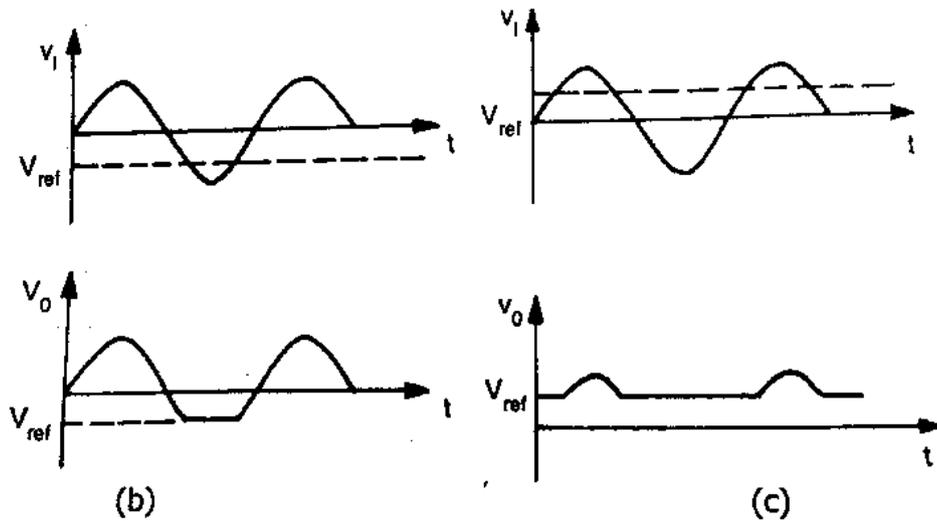
Fig. 3.47 Input-output waveforms for negative and positive V_{ref}

10. CLAMPERS

18. With circuit diagram explain the op- amp applications of clamper. (May – 14, Dec – 14, May – 17)

(or)

Elaborate with neat circuit diagram, and input/ output waveforms, the operation of peak clamper. (Nov/Dec 2019) (6)

→ The clamper is also known as d.c. inserter or restorer. The circuit is used to add a desired d.c. level to the output voltage.

→ In other words, the output is clamped to a desired d.c. level. If the clamped d.c. level is positive, it is called positive clamper.

→ Similarly if the clamped d.c. level is negative, the clamper is called negative clamper.

→ Fig. 48 shows a clamper with a variable positive d.c. voltage applied at the (+) input terminal.

→ This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper.
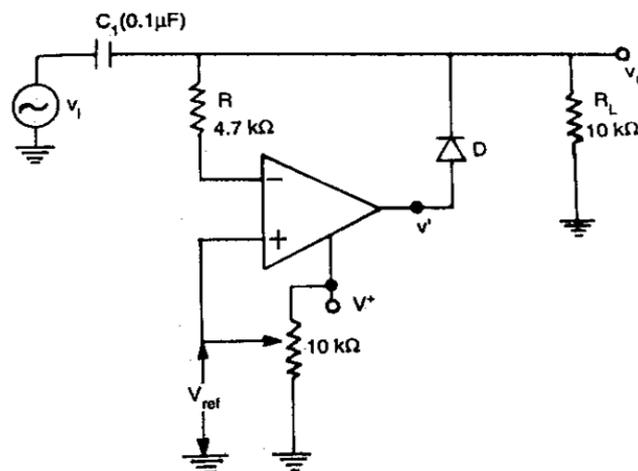
Fig. 3.48 Peak Clamper Circuit

→ The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively.

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→ Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased.

→ The circuit operates as a voltage follower and therefore output voltage $v_0 = + V_{ref}$.

→ Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal.

→ During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m.

→ However, during the positive half cycle of v_i, diode D is reverse biased. The capacitor retains its previous voltage V_m.

→ Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$.

→ The total output voltage is, therefore, $V_{ref} + v_i + V_m$.

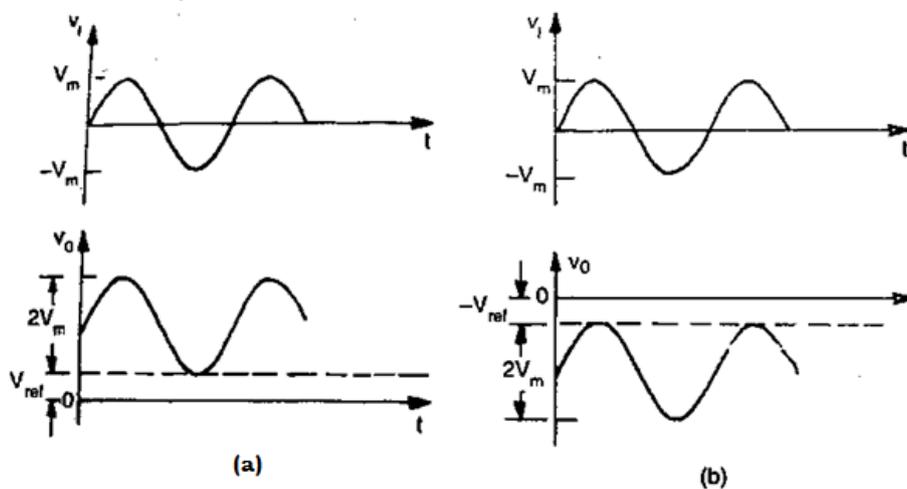→ The input and output waveforms are shown in Fig.3.49 (a).

Fig. 3.49 (a) Waveforms for + V_{ref} (b) Waveforms or – V_{ref}

→ It is possible to obtain negative peak clamping by reversing the diode D and using a negative reference voltage $–V_{ref}$.

→ The expected waveforms are shown in Fig.3.49 (b). The resistor R is used for protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the d.c. supply voltages are switched off.

11. PEAK DETECTORS

19. Explain the following application of operational amplifier as a peak detector. (May – 14, Dec – 14)

→ The function of a peak detector is to compute the peak value of the input.

→ The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor.

→ If a higher peak signal value comes along, this new value is stored.

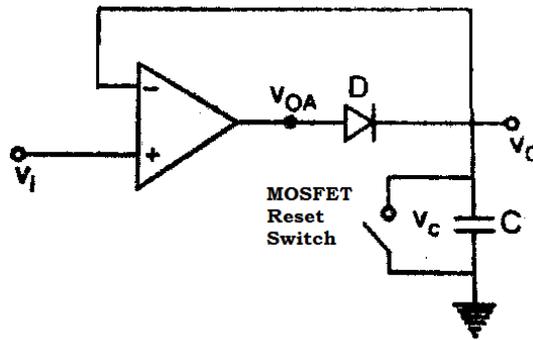→ The highest peak value is stored until the capacitor is discharged.

Fig. 3.50 Positive peak detector

→ Consider the circuit of Fig.3.50. When input v_i exceeds v_C, the voltage across the capacitor, the diode D is forward biased and the circuit becomes a voltage follower.

→ Consequently, the output voltage v_0 follows v_i as long as v_i exceeds v_C.

→ When v_i drops below v_C, the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than v_C.

→ Fig. 51 shows the voltage wave shape for the positive peak detector.
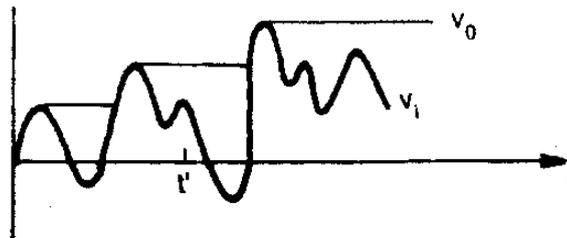
Fig. 3.51 Output v_0 corresponding to arbitrary input v_i

→ It may be noted that the peak at time t' is missed, the reason is obvious.

→ The circuit can be reset, that is, capacitor voltage can be made zero by connecting a lower leakage MOSFET switch across the capacitor.

→ The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode.

→ Peak detectors find application in test and measurement instrumentation as well as in amplitude modulation (AM) communication.

12. <u>S/H CIRCUIT</u>

20. Draw sample and hold circuit and explain its operation. (Dec – 14, 15) (8)

→ A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again.

→ This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems.

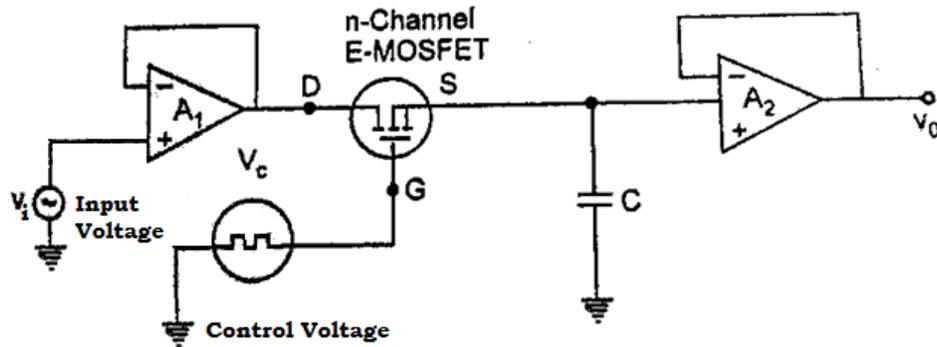→ One of the simplest practical sample and hold circuit configuration is shown in Fig.3.52.

Fig. 3.52 Sample and Hold Circuit

→ The n-channel E-MOSFET works as a switch and is controlled by the control voltage v_C and the capacitor C stores the charge.

→ The analog signal v_i to be sampled is applied to the drain of E-MOSFET and the control voltage v_C is applied to its gate.

→ When v_C is positive, the E-MOSFET turns **on** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_0 + r_{DS} (on)] C$.

→ Here R_0 is the output resistance of the voltage follower A_1 and r_{DS} (on) is the resistance of the MOSFET when **on**.

→ Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2.
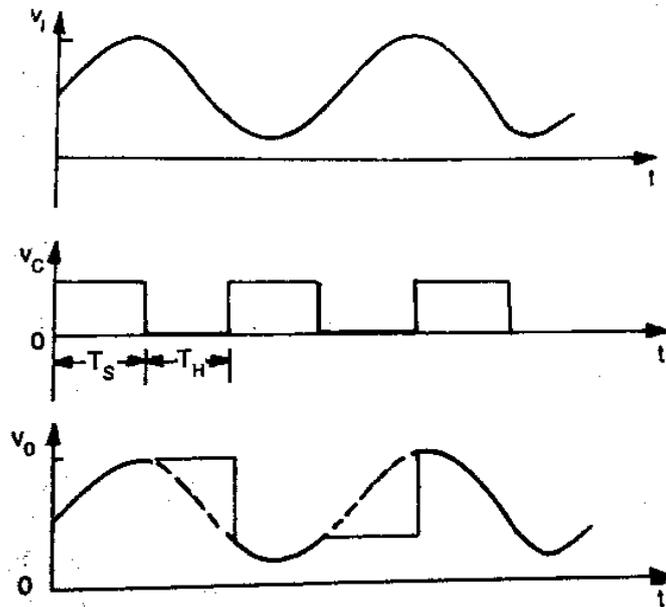
→ The waveforms are as shown in Fig.3.53.

Fig. 3.53 Input and Output Waveforms

→ During the time when control voltage v_C is zero, the E-MOSFET is **off**.

→ The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge.

→ The capacitor holds the voltage across it.

→ The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period.

→ The time period T_H of v_C during which the voltage across the capacitor is held constant is called hold period.

→ The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform.

→ A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

→ Specially designed sample and hold 108 of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available.
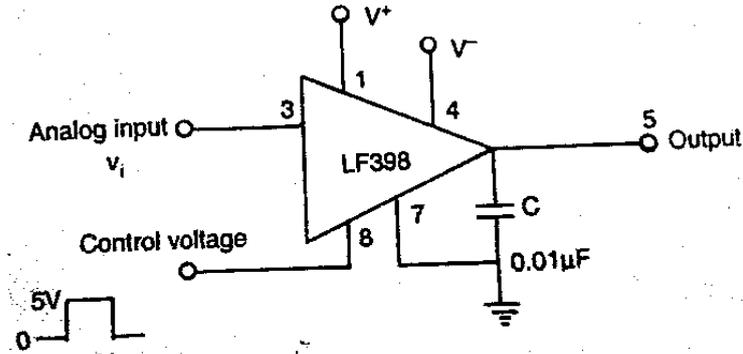

Fig. 3.54 Typical Connection Diagram

→ A typical connection diagram of the LF398 is shown in Fig. 3.54. It may be noted that the storage capacitor C is connected externally.

13. D/A CONVERTERS

21. With the circuit of neat diagram explain the operation of R/2R D/A converter. (May-15) (8)

(or)

With the circuit diagram explain the working principle of R-2R converter and binary weighted converter. (Nov-17) (13)

(or)

Discuss the application of Op-amps, with necessary equivalent circuits and expressions for D/A converters (Apr/May 2019)

→ Digital to analog converters converts digital signals into analog signals.
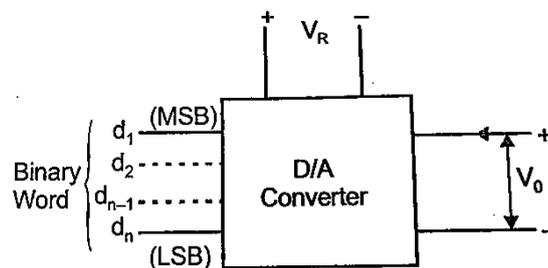

Fig. 3.55 Schematic diagram of a DAC

→ The output voltage of n-bit digital to analog converter is given by,

$$V_o = V_R (d_1 2^{-1} + d_2 2^{-2} + \cdots \ldots \ldots \ldots \ldots + d_n 2^{-n})$$

where,

V_R = Reference voltage

$d_1, d_2, \ldots \ldots \ldots, d_n$ = n – bit binary word

d_1 = MSB with weight of $V_R/2$

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d_2 = LSB with weight of $V_R/2^n$

13.1 Types:

1. Binary weighted resistor DAC
2. R-2R ladder
3. Inverted R-2R ladder.

13.1.1 Binary Weighted Resistor DAC:

→ The binary weighted resistor DAC uses operational amplifier to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors 2R, 4R, 8R … 2^nR.
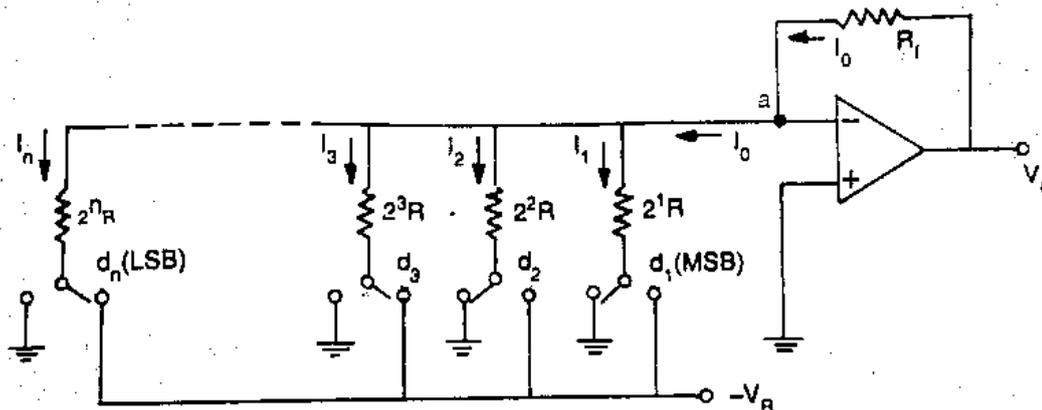

Fig. 3.56 A simple weighted resistor DAC

→ The switch positions are controlled by digital inputs. When the digital input is one, the corresponding switch is closed and digital input is zero.

→ The operational amplifier is used as a summing amplifier. Due to the high input impedance of op-amp, summing current will flow through feedback resistor R_f.

→ The total current is,

$$I_T = I_1 + I_2 + I_3 \dots \dots + I_n$$

→ The output voltage is the voltage drop across R_f and it is given as,

$$V_0 = -I_T R_f$$

$$V_0 = -(I_1 + I_2 + I_3 \dots \dots + I_n)R_f$$

$$V_0 = -(d_1 \frac{V_R}{2R} + d_2 \frac{V_R}{4R} + d_3 \frac{V_R}{8R} \dots \dots + d_n \frac{V_R}{2^n R})R_f$$

$$V_0 = -\frac{V_R}{R}(d_1 2^{-1} + d_2 2^{-2} + \dots \dots \dots \dots \dots + d_n 2^{-n})R_f$$

When $R_f = R$, the output voltage becomes

$$\boldsymbol{V_o = -V_R(d_1 2^{-1} + d_2 2^{-2} + \dots \dots \dots \dots \dots + d_n 2^{-n})}$$

→ From this equation, analog output voltage is directly proportional to the input digital data.

→ The analog output voltage is therefore positive staircase as shown in Fig. 57 for a 3-bit weighted resistor DAC.

→ It may be noted that,

   ❖ Although the op-amp in Fig. 3.56 is connected in inverting mode, it can also be connected in non-inverting mode.

   ❖ The op-amp is simply working as a current to voltage converter.

53

❖ The polarity of the reference voltage is chosen in accordance with the type of the switch used.

→ The accuracy and stability of a DAC depends on the accuracy of the resistors and the tracking of each other with temperature.
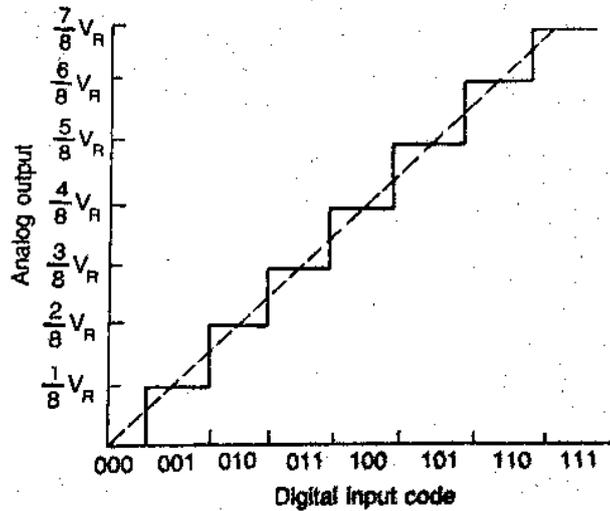

Fig. 3.57 Transfer characteristics of a 3-bit DAC

Disadvantages:

❖ Wide range of Resistor values is required.

❖ It is observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the resistance value increases.

13.1.2 R-2R ladder DAC:

22. with neat diagram, explain the working principle of R-2R ladder type DAC. (May – 17) (8)

→ R-2R ladder D/A converters use only two resistor values.

→ This avoids resistance spread drawback of binary weighted D/A converter.

→ Like binary resistor DAC, it also uses shunt resistors to generate n binary weighted currents; it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC.

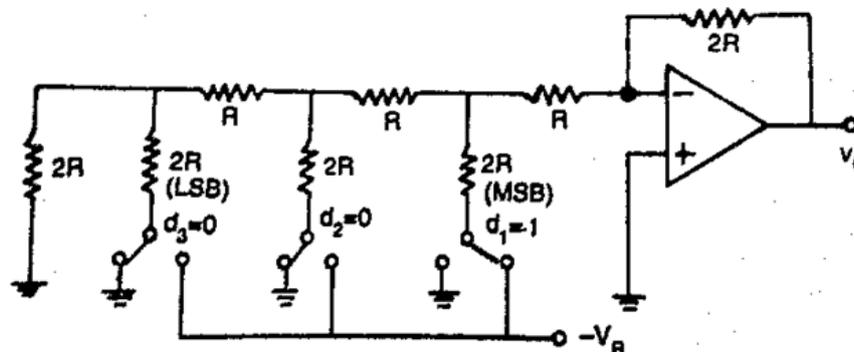→ Voltage scaling requires an additional set of voltage dropping series resistance between adjacent nodes.

Fig. 3.58 R-2R ladder DAC

→ Each bit of the binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground.

→ Both the positions of switches are at ground potential, the current flowing through resistance is constant and it is independent of switch position.

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$$I_1 = {V_R}/{2R}$$

$$I_2 = \frac{{V_R}/{2}}{2R} = \frac{V_R}{4R}$$

$$I_3 = \frac{{V_R}/{4}}{2R} = \frac{V_R}{8R}$$

$\rightarrow$ The output voltage V_0 is,

$$V_0 = -I_T R_f$$

$$V_0 = -R_f(I_1 + I_2 + I_3 \dots \dots + I_n)$$

$$V_0 = -\left[d_1 \frac{V_R}{2R} + d_2 \frac{V_R}{4R} + d_3 \frac{V_R}{8R} \dots \dots + d_n \frac{V_R}{2^n R}\right]$$

$$V_0 = -V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \cdots \dots \dots \dots \dots + d_n 2^{-n})$$

$\rightarrow$ When $R_f = R$, the output voltage is,

$$\boldsymbol{V_o = -V_R (d_1 2^{-1} + d_2 2^{-2} + \cdots \dots \dots \dots \dots + d_n 2^{-n})}$$

14 A/D CONVERTERS USING OP-AMPS

23. Explain the successive approximation type ADC with its characteristics. (Dec – 12) (May-18) (9)(Nov/Dec 2019) (8, 11)

(or)

Explain the principle of operation of A/D converter. (May – 11) (8)

(or)

Explain the basic operation of A/D converter utilizing D/A converter. (May – 15) (8)

(or)

Discuss the application of Op-amps, with necessary equivalent circuits and expressions for A/D converters (Apr/May 2019)

$\rightarrow$ An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form is known as analog to digital converter.

14.1 Types of A/D Converters:
- ❖ Dual Slope A/D Converter.
- ❖ Successive Approximation A/D Converter.
- ❖ Flash A/D Converter.
- ❖

14.1.1 Successive Approximation Type Analog to Digital Converter:

$\rightarrow$ An eight bit converter which requires 8 clock pulses to obtain digital output.

$\rightarrow$ It consists of successive approximation register (SAR), operational amplifier, and D/A converter.

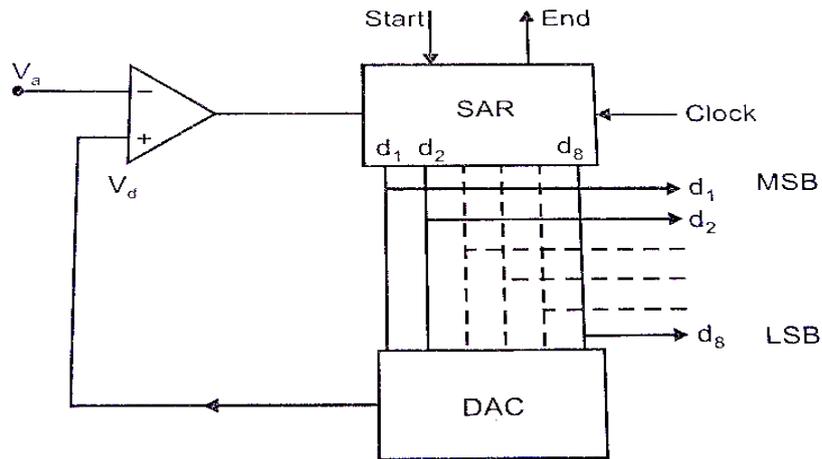$\rightarrow$ SAR is used to find the required value of each bit by trial and error.

Fig. 3.59 Functional diagram of Successive Approximation ADC

$\rightarrow$ When start command is received the SAR sets $d_1=1$ for eight bit code and all other to zero.

$\rightarrow$ The output V_d from DAC is compared with analog input V_a. If $V_a>V_d$, then 10000000 is less than correct digital representation.

$\rightarrow$ The MSB will remains at '1' and next bit is made '1' and further tested.

$\rightarrow$ When $V_a<V_d$, zero is introduced to next LSB and process repeats. It repeats till it receives EOC command.

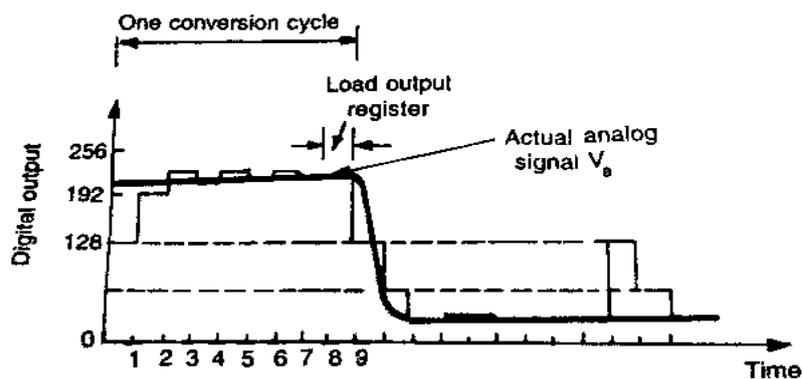| CORRECT SIGNAL	CONVERSION	OUTPUT
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010100	0
	11010100	

Fig. 3.60 The D/A output voltage is seen to become successively closer to the actual analog input voltage

14.1.1.1 Advantages:

❖ High resolution.
❖ It is very versatile.
❖ High Speed.

14.1.1.2 Application:

❖ Data acquisition systems.

24. Explain the following application of operational amplifier as a Flash Type A/D Converter.(8) (Dec – 16)

→ It is the simplest, fastest and most expensive technique.

→ It consists of resistive divider network, 8 comparators and a 8-line to 3-line encoder for a 3 – bit A-D converter.

→ If both inputs were of equal voltage a small amount of hysteresis is built into comparator.

→ The main purpose is to compare the analog input voltage V_a with each of the node voltage.

→ The resistor voltage available at node is divided equally between V_R and ground.

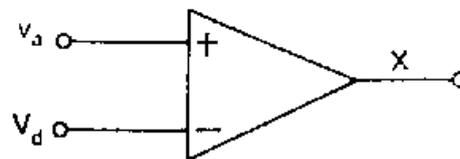| Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

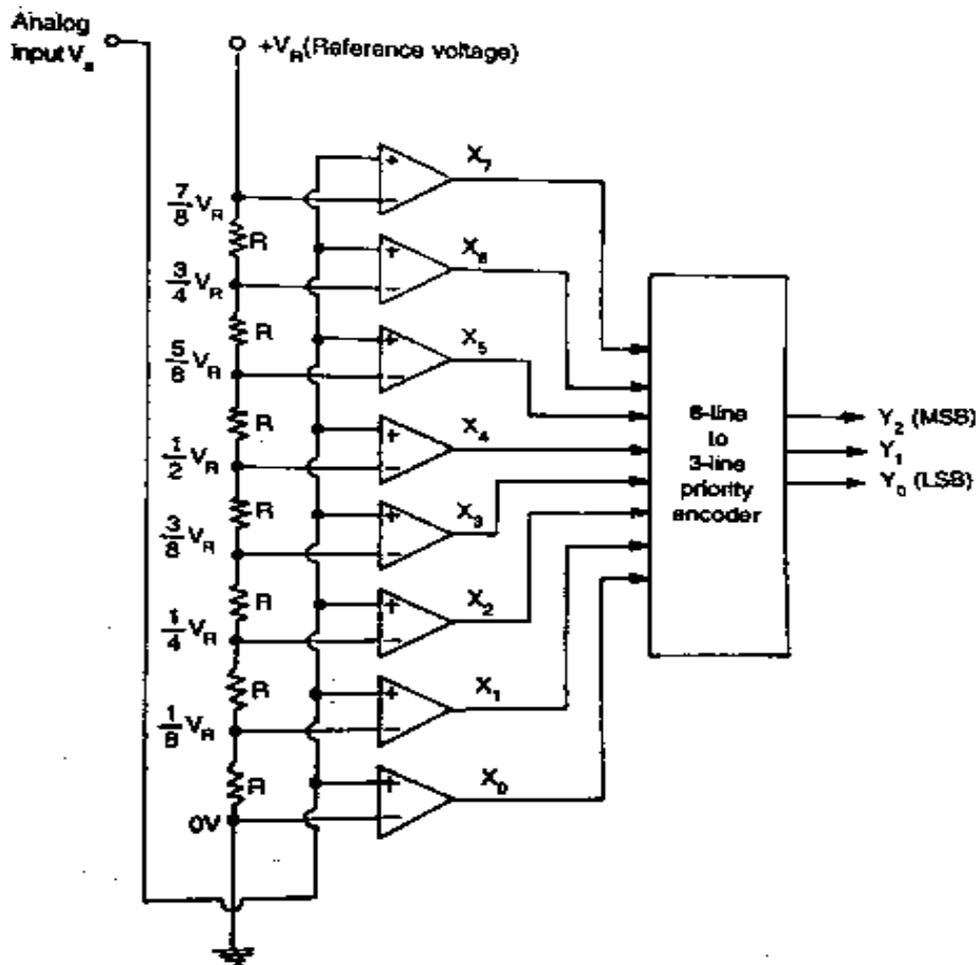**Fig. 3.62 Comparator and its truth table**

Fig. 3.61 Flash type A/D Converter

→ The truth table for the flash type A-D converter is shown in Fig.3.63.

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→ The conversion speed is high as the conversion takes place simultaneously rather than sequentially.

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 63 Truth table for Flash type A/D Converter

→ In general, the number of comparators required is $2^n - 1$ where n is the desired number of bits.

14.1.2.1 Advantages:
  ❖ High speed operation conversion takes place.
  ❖ Conversion time is 100ns or less.

14.1.2.2 Disadvantages:
  ❖ Designing becomes complex for higher value.
  ❖ For each added bit, size of comparator is doubled.

14.1.2.3 Applications:
  ❖ High speed fiber optic communication, digital storage oscilloscope.

14.1.3 Stair case ramp type:
  → A stair case ramp type converter consists of comparator, DAC, AND gate and a counter.
  → The basic principle is that the input signal V_a is compared with an internal stair case voltage V_d, generated by a series circuit consisting of a pulse generator (clock), a counter counting the pulses and a digital to analog converter, converting the counter output into a d.c. signal.
  → As soon as V_d is equal to V_a, the input comparator closes a gate between the clock and counter, the counter stops and its output is shown on the display.
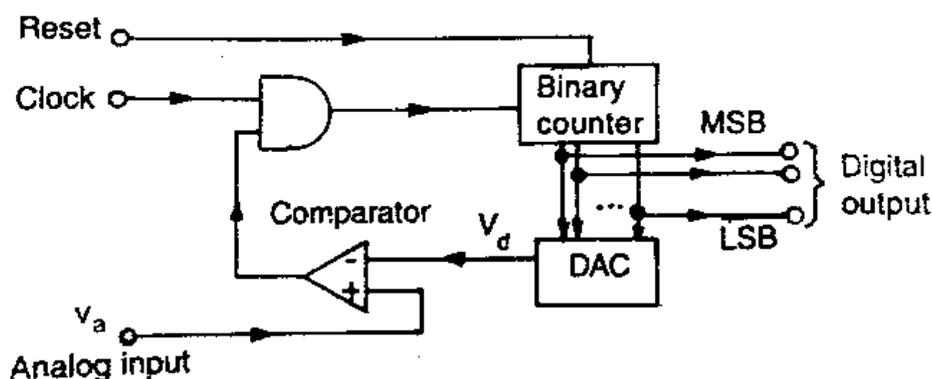

Fig. 3.64 Counter type A/D Converter

14.1.3.1 Operation:
  → The clock generates pulses continuously. At the start of a measurement, the counter is reset at 0 so that the output of the digital to analog converter is also zero.
  → If V_a is not equal to zero, the input comparator applies an output voltage that opens the gate so that the clock pulses are passed on to the counter through gate.

→ The counter starts counting and the DAC starts to produce an output voltage increasing one small step at each count of the counter.

→ The result is a stair case voltage applied to the second input of the comparator.

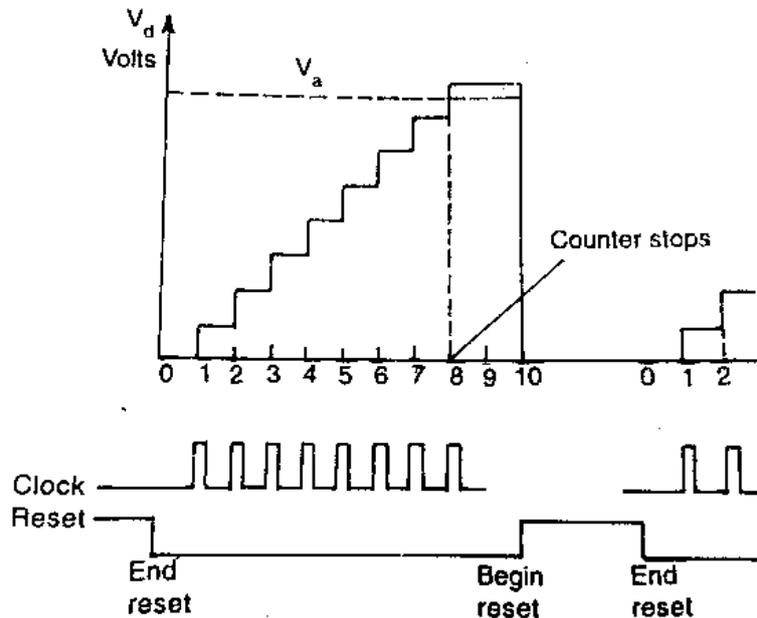→ This process continues until the staircase voltage is equal to or slightly greater than the input voltage V_a.

Fig. 3.64 D/A output staircase waveform

→ When $V_d \geq V_a$, the output voltage of the input comparator changes state or polarity, so that the gate closes and counter is stopped.

→ The display unit shows the result of the count.
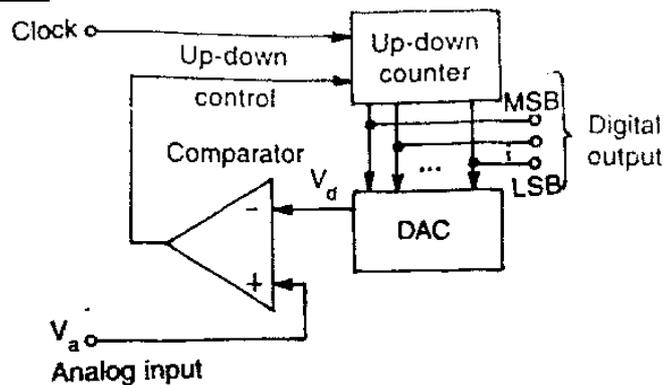
14.1.4 Servo tracking ADC:

Fig. 3.65 A Tracking A/D Converter

→ It has an up-down counter which counts in both directions.

→ Analog output of DAC is V_d which is compared with analog input V_a.

→ If $V_a > V_d$ output of comparator becomes 1 and counter counts up for each incoming clock pulse with increased output and the counter counts one up till the maximum value.

→ If the maximum value is attained it starts to count one down till the LSB value.

→ It repeats back forth for each increase in value as analog input changes slowly for rapid increase in input, it cannot able to change and becomes error.
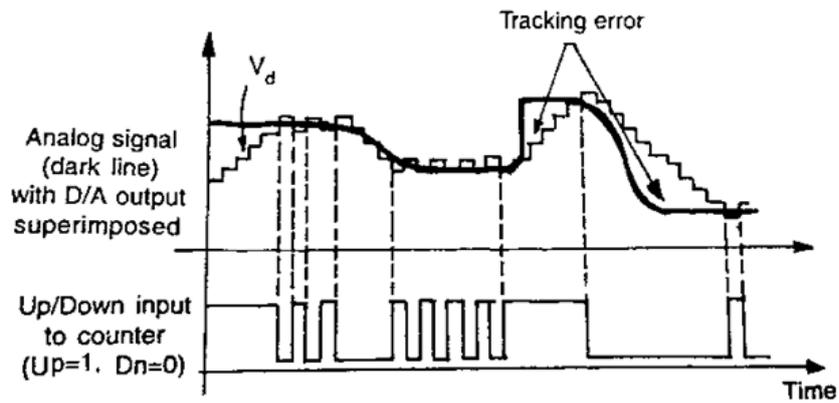
59

Fig. 3.66 Waveforms associated with tracking A/D Converter

14.1.4.1 Advantage:
- ❖ The process is simple.

14.1.4.2 Disadvantage:
- ❖ It needs time.

14.1.5 Dual slope A/D conversion:

25. Explain the operation of dual slope ADC. (May – 14, Dec – 14)

→ It is an indirect method.

→ An analog voltage and a reference voltage are converted into time periods by an integrator and then measured by a counter.

→ The speed of this conversion is slow but the accuracy is high.

14.1.5.1 Construction:

→ It consists of an integrator (ramp generator), comparator, binary counter, output latch and a reference voltage.

→ The ramp generator input is switched between the analog input voltage V_i and a negative reference voltage $– V_R$.
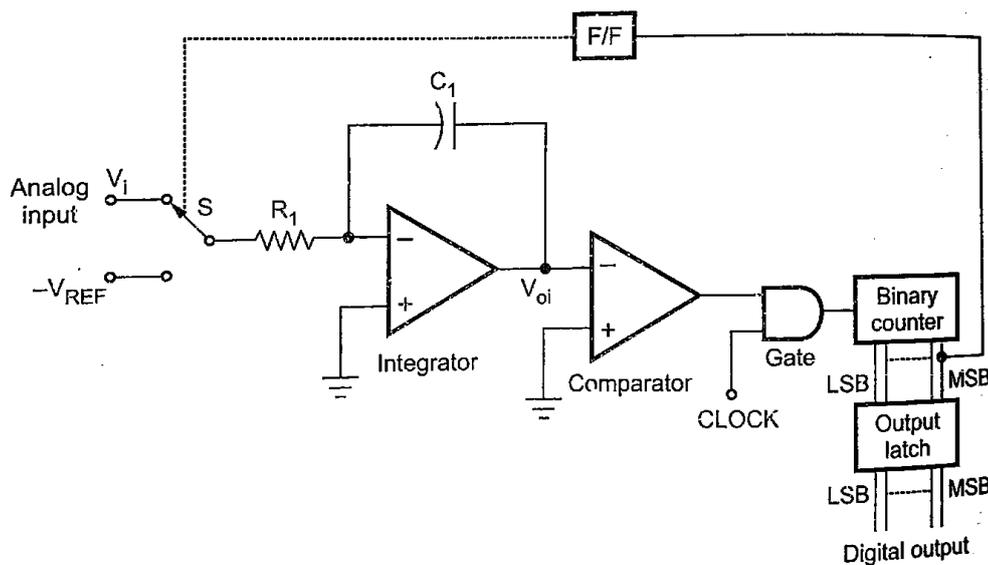

Fig. 3.67 Functional diagram of Dual Slope ADC

→ The analog switch is controlled by the MSB of the counter.

→ When the MSB is logic 0, the voltage being measured is connected to the ramp generator input.

→ When MSB is logic 1, the negative reference voltage is connected to the ramp generator.

→ At time t=0, analog switch S is connected to the analog input voltage V_i the analog input voltage integration begins.

→ The output voltage of the integrator is,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i \, dt = \frac{-V_i \, t}{R_1 C_1}$$

where $R_1 C_1$ is the integrator time constant.

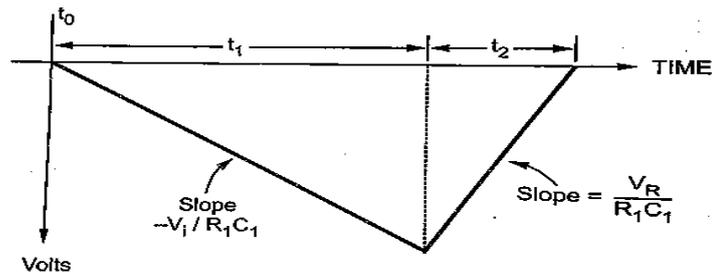V_i is assumed constant over the integration time period.

Fig. 3.68 Integrated output waveform for the dual slope ADC

→ At the end of 2^n clock periods MSB of the counter goes high.

→ As a result the output of the flip-flop goes high, which causes analog switch S to be switched from V_i to $-V_R$.

→ At this very same time the binary counter which has gone through its entire count sequence is reset.

→ The negative input voltage $-V_R$ connected to the input of integrator causes the integrator output to ramp positive.

→ When integrator output reaches zero, the comparator output voltage goes low, which disables the clock AND gate.

→ This stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2.

→ The charge voltage is equal to discharge voltage,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_i t_1 = V_R t_2$$

$$t_2 = \left(\frac{V_i t_1}{V_R} \right)$$

Digital output= (counts/second) t_2 Digital output= (counts/ second) $\left(\frac{V_i t_1}{V_R} \right)$

14.1.5.2 Advantages:

❖ It is highly accurate, its cost is low.

❖ It is immune to temperature caused variations in R_1 and C_1.

14.1.5.3 Disadvantage:

❖ Speed is low.

Functional block – characteristics of 555 Timer and its PWM application - IC – 566 voltage controlled oscillator IC – 565 phase lock loop IC – AD 633 Analog multiplier ICs.

Part – B – 16Mark Questions

4.1 FUNCTIONAL BLOCK

1. **Sketch the functional block diagram of IC555 and explain their working principle. [May/June 2012][April/May 2017][Nov/Dec 2015] (8)**

(or)

Explain the functional block diagram of NE 561 phase locked loop. (May-2018) (7)

(or)

Explain the functional block and characteristics of IC 555 timer with its PWM application. [Apr/May 2019] 13 marks

(or)

Demonstrate with neat functional diagram, the working of 555 IC timer. Develop the expression for pulse with of rectangular output pulse. Nov/Dec 2019 (13 marks)

4.1.1 Introduction:

→ The 555 timer is a highly stable device for generating accurate time delay or oscillation.

→ Signeta Corporation first introduced this device as the SE555/NE555.

→ It is available in two package styles, 8 – pin circular style, TO – 99 can or 8 – pin mini DIP or as 14 –pin DIP.

→ The 556 timer contains two 555 timers and is a 14 – pin DIP.

→ There is also available counter timer such as Exar's XR – 2240 which contains a 555 timer plus a programmable binary counter in a single 16 – pin package.

→ A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.
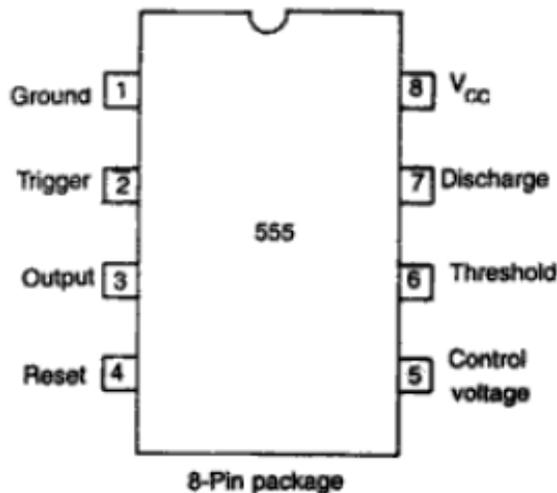

Figure 1: Pin Diagram

→ The 555 timer can be used with supply voltage in the range of + 5V to +18V and can drive load till 200 mA.

→ It is compatible with both TTL and CMOS logic circuits.

→ Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications.

→ Various applications include oscillator, pulse generator, ramp and square wave generator mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

4.1.2 DESCRIPTION OR FUNCTIONAL DIAGRAM:

→ Fig. 1 gives the pin diagram and Fig. 2 gives the functional diagram for 555 IC timers.

→ Referring to Fig.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{CC} to the upper comparator (UC) and (1/3) V_{CC} to the lower comparator (LC), where V_{CC} is the supply voltage.

→ Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval.

→ It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5).

→ In applications where no such modulation as intended it is recommended by manufacturers that a capacitor (0.01 MF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.
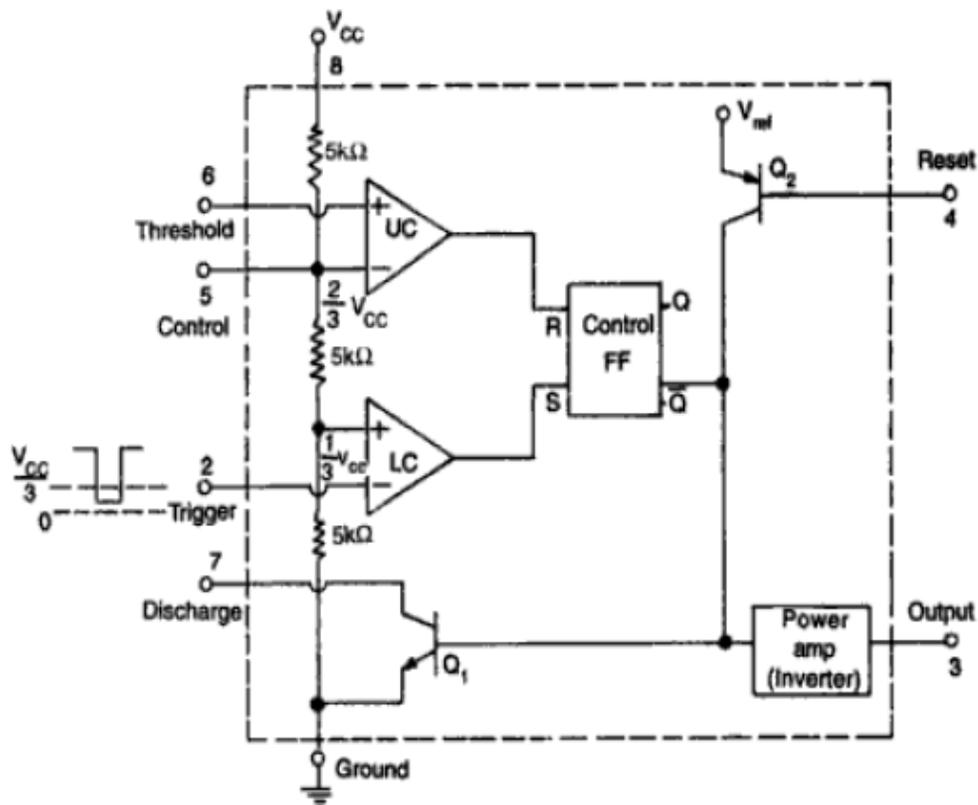

Figure 2: Functional diagram of 555 timers

→ In the standby (stable) state, the output $\bar{Q}$ of the central flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter.

→ A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{CC}/3$).

→ At the negative going edge of the trigger as the trigger passes through ($V_{CC}/3$), the output of the lower comparator goes HIGH and sets the FF (Q = 1, $\bar{Q}$ = 0).

→ During the positive excursion when the threshold voltage at pin 6 passes through (2/3) V_{CC}, the output of the upper comparator goes HIGH and resets the FF (Q = 0, $\bar{Q}$ = 1).

→ The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

→ This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}.

→ The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1.

→ The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

4.2 CHARACTERISTICS OF 555 TIMER AND ITS PWM APPLICATION

4.2.1   MONOSTABLE OPERATION

2. **With neat diagrams, explain the working of IC555 in mono stable mode. (8)**

→ Figure 3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 4.

→ In the standby state, FF holds transistor Q_1ON, thus clamping the external timing capacitor C to ground.

→ The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $\bar{Q}$ = 0.

→ This makes the transistor Q_1OFF and the short circuit across the timing capacitor C is released.

→ As $\bar{Q}$ is LOW, output goes HIGH (= V_{CC}). The timing cycle now begins.

→ Since C is unclamped, voltage across it rises exponentially through R towards V_{CC} with a time constant RC as in Fig. 5(b).

→ After a time period T, the capacitor voltage is just greater than (2/3) V_{CC} and the upper comparator resets the FF, that is, R = 1, S = 0 (assuming very small trigger pulse width).

→ This makes $\bar{Q}$ = 1, transistor Q_1 goes ON (i.e. saturates), thereby, discharging the capacitor C rapidly to ground potential.

→ The output returns to the standby state or ground potential as shown in Fig. 5(c).
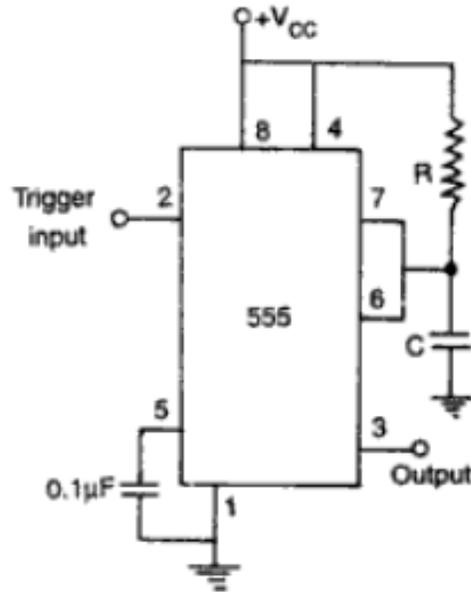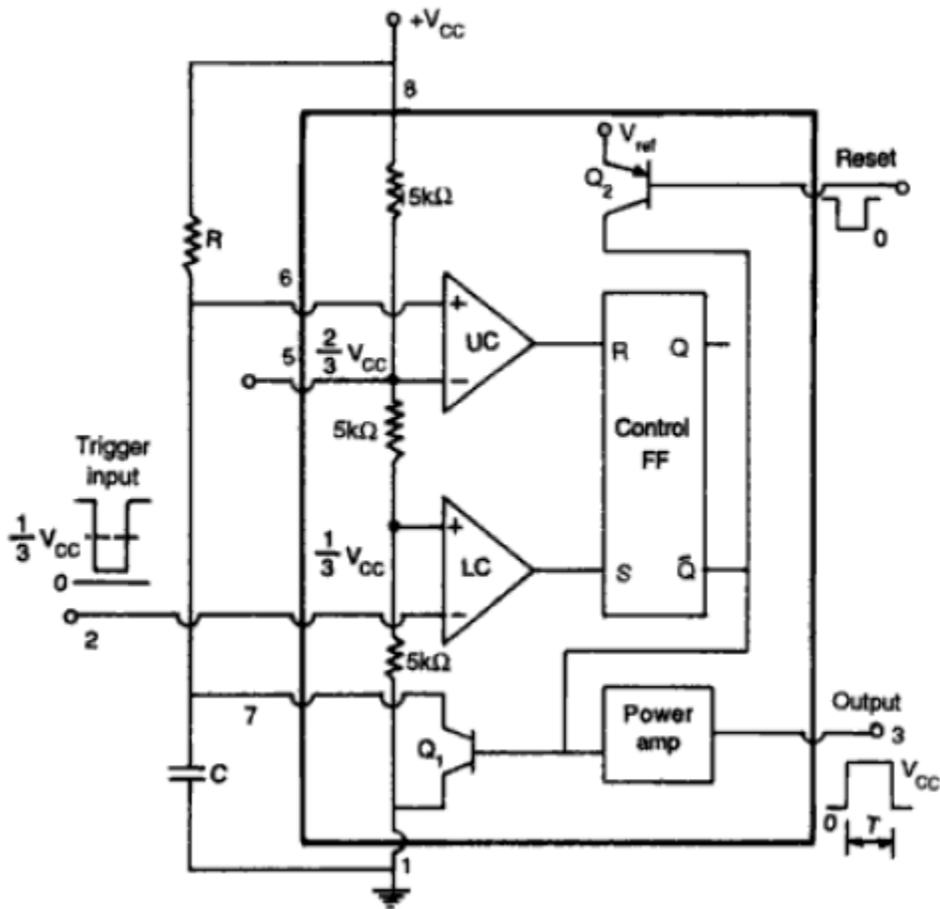
Figure 3: Monostable multivibrator

Figure 4: Timer in monostable operation with functional diagram

→ The voltage across the capacitor as in Fig. 5(b) is given by

4

$$V_c = V_{CC}\left(1 - e^{-t/RC}\right) \rightarrow (1)$$

At t = T, v_c = (2/3) V_{CC}

$$\therefore \frac{2}{3}V_{CC} = V_{CC}\left(1 - e^{-t/RC}\right)$$

or,   T = RC ln (1/3)

or,   T = 1.1 RC (sec)→ (2)

→ It is evident from Eq. (2) that the timing interval is independent of the supply voltage.

→ It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C.

→ Any additional trigger pulse coming during this time will not change the output state.

→ However, if a negative going reset pulse as in Fig. 5(d) is applied to the reset terminal (pin – 4) during the timing cycle, transistor Q_2 goes OFF, Q_1 becomes ON and the external timing capacitor C is immediately discharged.

→ The output now will be as in Fig. 5(e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ON Q_1 immediately and thereby avoid the propagation delay through the FF.

→ Now, even if the reset is released, the output will still remain LOW until a negative going trigger pulse is again applied at pin 2.
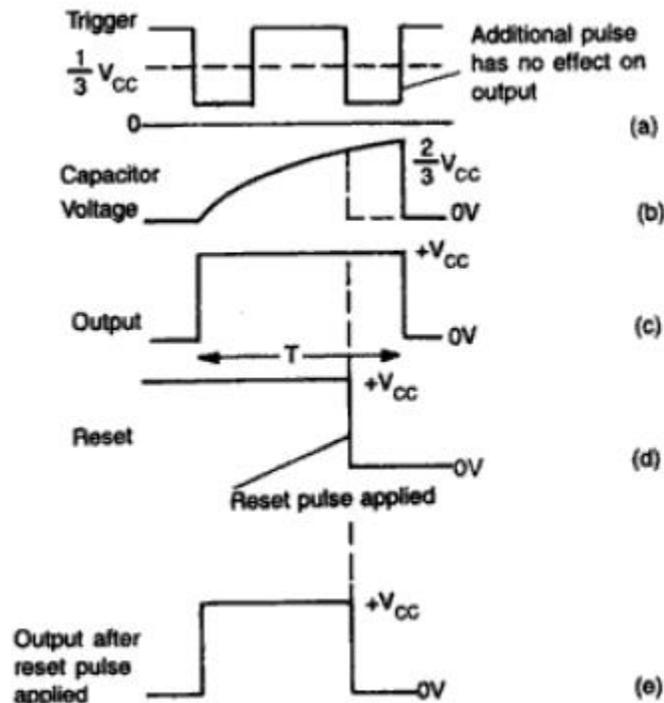

Figure 5: Timing pulses

→ Fig. 6 shows a graph of the various combinations of R and C necessary to produce a given time delay.
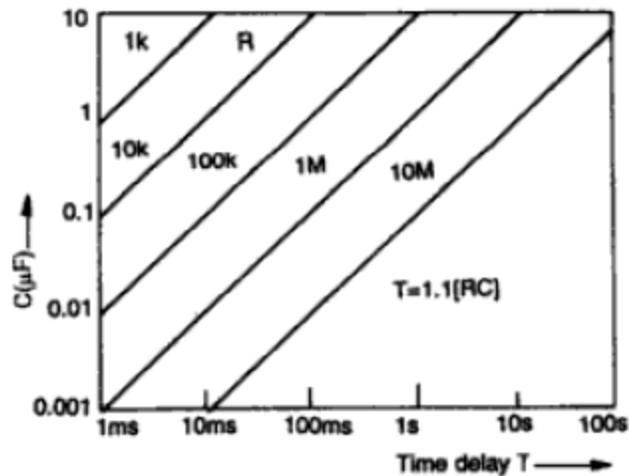
Figure 6: Graph of RC combinations for different time delays

→ Sometimes the monostable circuit of Fig.3 mis-triggers on positive pulse edges, even with the control pin bypass capacitor.

→ To prevent this, a modified circuit as shown in Fig.7 is used.

→ Here the resistor and capacitor combination of 10 kΩ and 0.001 µF at the input forms a differentiator.

→ During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7V.
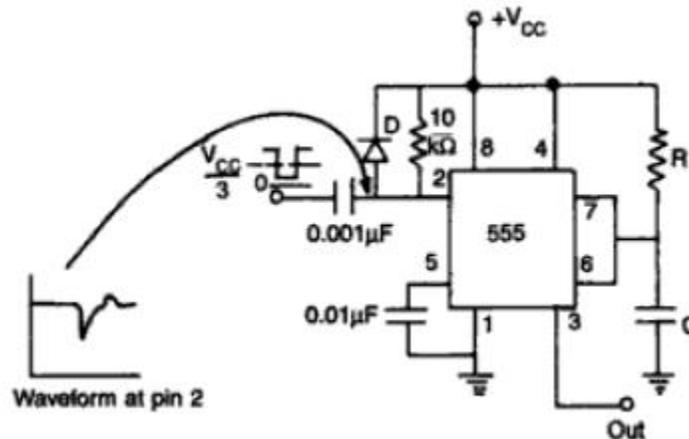
Figure 7: Modified monostable circuit

4.2.2 Applications In Monostable Mode

3. Discuss in detail the applications of Monostable Mode?

4.2.2.1 Missing Pulse Detector

→ Missing pulse detector circuit using 555 timer is shown in Fig. 8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased.

→ The capacitor C gets clamped to few tenths of a volt (~ 0.7V). The output of the timer goes HIGH.

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→ The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses.

→ As long as the trigger pulse train keeps coming at pin 2, the output remains HIGH.

→ However, if a pulse misses, the trigger input is high and transistor Q is cut off. The 555 timer enters into normal state of monostable operation.

→ The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat.

→ It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.
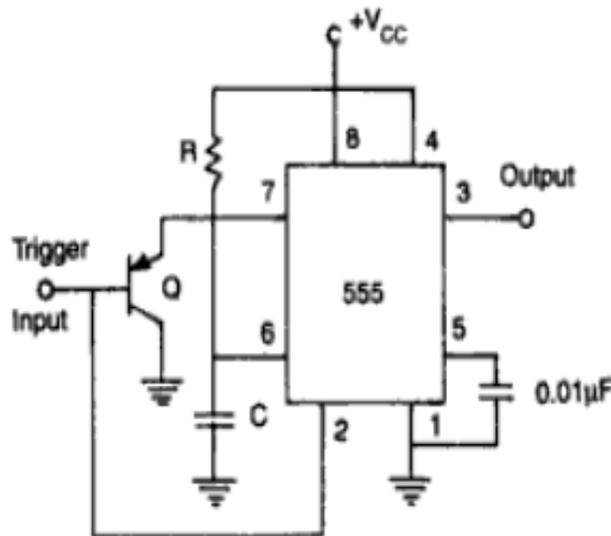
Figure 8: A missing pulse detector monostable circuit
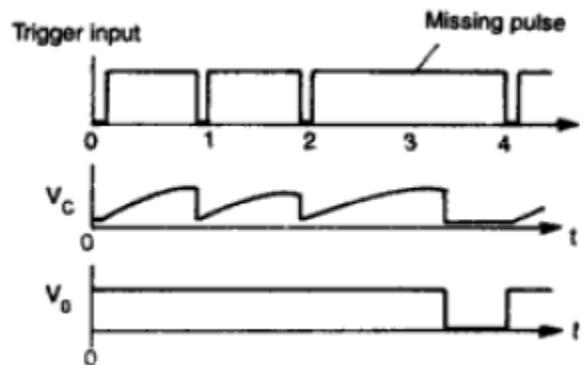
Figure 9: Output of missing pulse detector

4.2.2.2 Linear Ramp Generator

→ Linear ramp can be generated by the circuit shown in Fig. 10. The resistor R of the monostable circuit is replaced by a constant current source.

→ The capacitor is charged linearly by the constant current source formed by the transistor Q_3.

→ The capacitor voltage v_C can be written as,

7

$$v_C = \frac{1}{C}\int_0^t i\,dt \rightarrow (3)$$

→ Where, i is the current supplied by the constant current source. Further, the KVL equation can be written as,

$$\frac{R_1}{R_1 + R_2}V_{CC} - V_{BE} = (\beta + 1)I_B R_E \approx \beta I_B R_E = I_C R_E = iR_E \rightarrow (4)$$

→ Where, I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE mode and is very high.

Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E(R_1 + R_2)} \rightarrow (5)$$
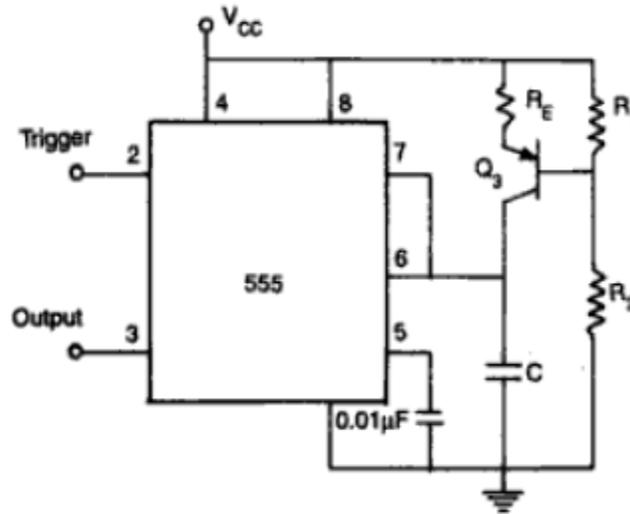
Figure 10: Linear ramp generator

→ Now putting the value of the current i in equation (3), we get,

$$v_C = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{CR_E(R_1 + R_2)} \times t \rightarrow (6)$$

→ At time t = T, the capacitor voltage v_c becomes (2/3) V_{CC}. Then we get,

$$\frac{2}{3}V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{CR_E(R_1 + R_2)} \times T \rightarrow (7)$$

→ This gives the time period of the linear ramp generator as,

$$T = \frac{(2/3)V_{CC}R_E(R_1 + R_2)C}{R_1 V_{CC} - V_{BE}(R_1 + R_2)} \rightarrow (8)$$

→ The capacitor discharges as soon as its voltage reaches (2/3) V_{CC} which is the threshold of the upper comparator in the monostable circuit functional diagram.

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→ The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 11.

→ The practical values can be noted as

$R_1 = 47$ kΩ $\qquad\qquad$ $R_2 = 100$ kΩ

$R_E = 2.7$ kΩ $\qquad\qquad$ $C = 0.1$ μF

$V_{CC} = 5$ V (any value between 5 to 18 V can be chosen)
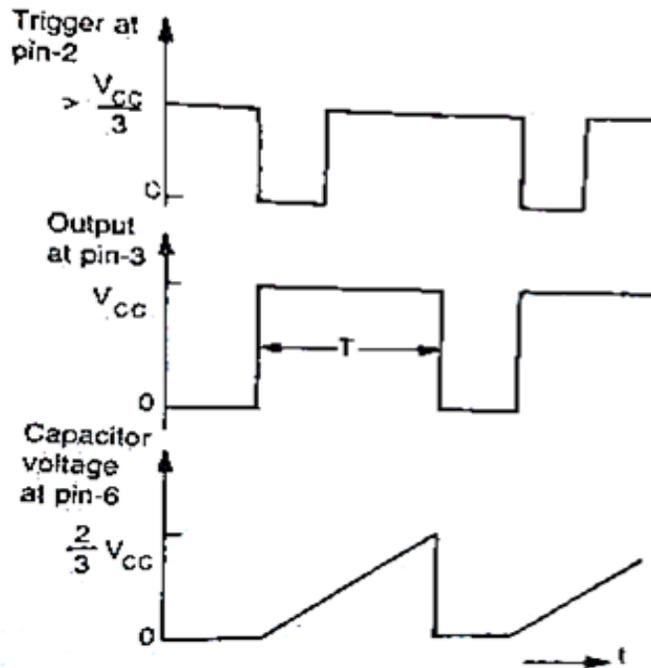
Figure 11: Linear Ramp generator output

4.2.2.3 <u>Frequency Divider:</u>

→ A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal.

→ The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 12.

→ The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay.

→ In this way, the outputs can be made integral fractions of the frequency of the input triggering square wave.

9
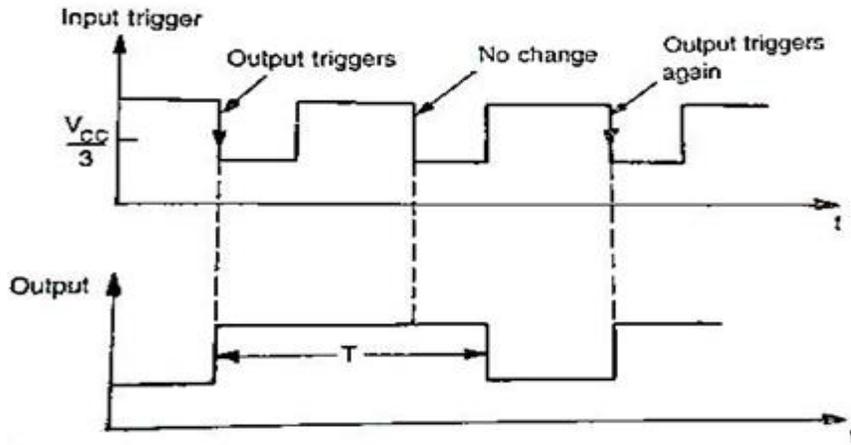
Figure 12: Frequency divider waveform

4.2.2.4 Pulse Width Modulation:

→ The circuit is shown in Fig. 13. This is basically a monostable multivibrator with a modulating input signal applied at pin – 5.

→ By the application of continuous trigger at pin – 2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin – 5.

→ The modulating signal applied at pin – 5 gets superimposed upon the already existing voltage (2/3) V_{CC} at the inverting input terminal of UC.

→ This in turn changes the threshold level of UC and the output pulse width modulation takes place.

→ The modulating signal and the output waveform are shown in Fig. 14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.
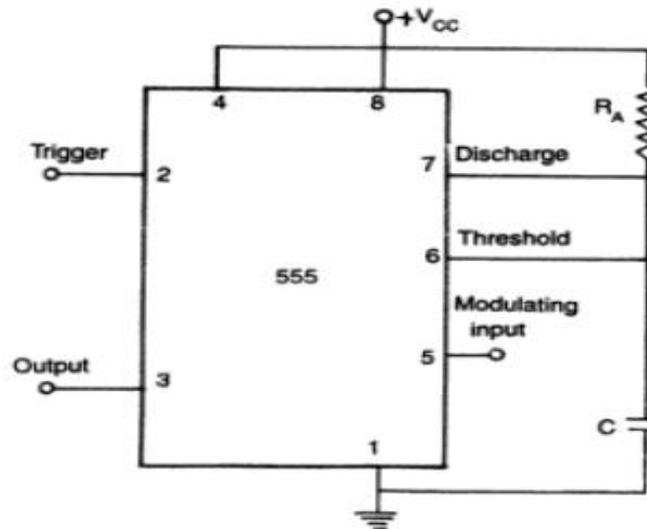
Figure 13: Pulse width modulator
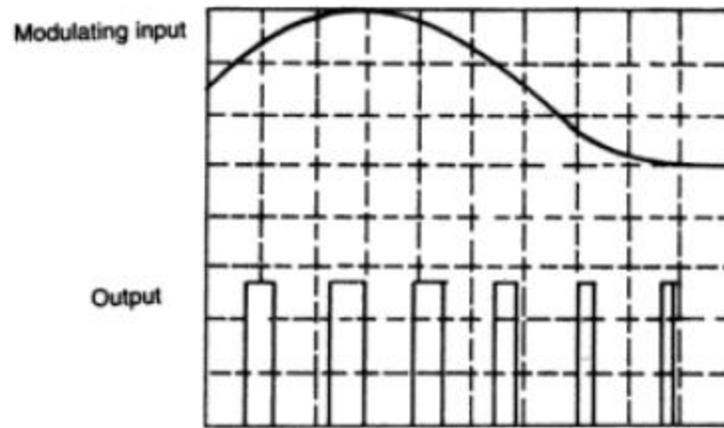
Figure 14: Pulse width modulator waveforms

4.2.3 ASTABLE OPERATION

> **4. With neat diagrams, explain the working of IC555 in Astable mode. (8) [May/June 2011] [April/May 2015]**

→ The device is connected for an Astable operation as shown in Fig. 15. For better understanding, the complete diagram of an Astable multivibrator with detailed internal diagram of 555 is shown in Fig. 16.

→ Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B.

→ Pin 7 of discharging transistor Q1 is connected to the junction of R_A and R_B. When the power supply V_{CC} is connected, the external timing capacitor C charges towards V_{CC} with a time constant $(R_A + R_B)C$.

→ During this time, output (pin 3) is high (equals V_{CC}) as Reset R = 0, Set S = 1 and this combination makes $\bar{Q} = 0$ which has unclamped the timing capacitor C.
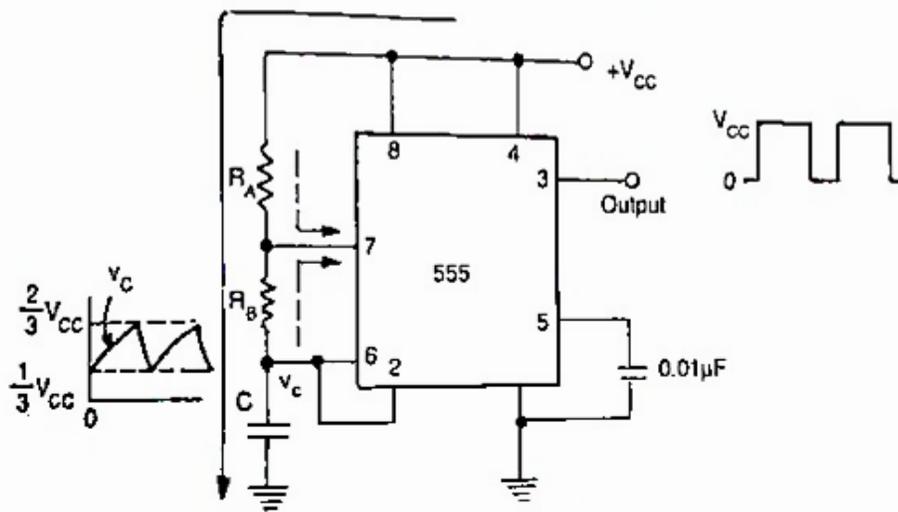
Figure 15: Astable multivibrator using 555 timer

11
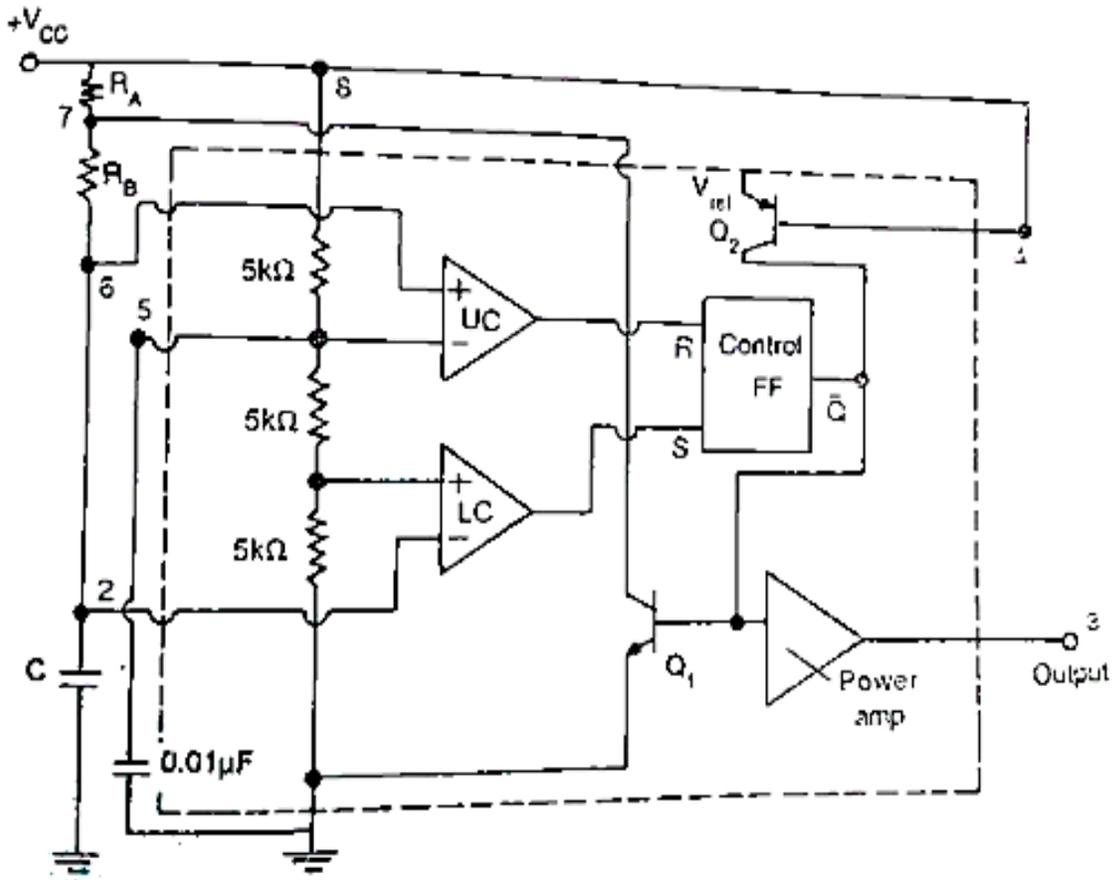
Figure 16: Functional diagram of astable multivibrator using 555 timer

→ When the capacitor voltage equals (2/3) V_{CC} the upper comparator triggers the control flip-flop so that $\bar{Q} = 1$.

→ This, in turn, makes transistor Q_1 ON and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant $R_B C$ (neglecting the forward resistance of Q_1).

→ Current also flows into transistor Q_1 through R_A.

→ Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1.

→ The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2 A is the maximum current through the ON transistor Q_1.

→ During the discharge of the timing capacitor C, as it reaches $V_{CC}/3$, the lower comparator is triggered and at this stage S = 1, R = 0, which turns $\bar{Q} = 0$.

→ Now $\bar{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively.

→ Fig. 17 shows the timing sequence and capacitor voltage wave form.

→ The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}.

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$\rightarrow$ It may be calculated as follows:
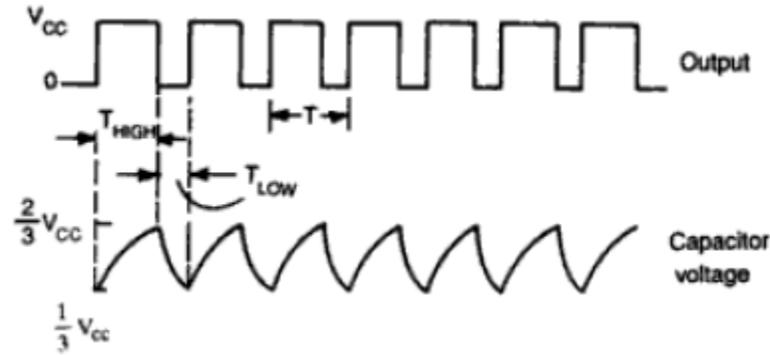
Figure 17: Timing sequence of Astable multivibrator

$\rightarrow$ The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} is given by,
$$v_C = V_{CC}(1 - e^{-t/RC})$$

$\rightarrow$ The time taken by the circuit to charge from 0 to (2/3) V_{CC} is,
$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-t_1/RC}) \rightarrow (9)$$

or, $t_1 = 1.09$ RC

and the time t_2 to charge from 0 to (1/3) V_{CC} is,
$$\frac{1}{3}V_{CC} = V_{CC}(1 - e^{-t_2/RC}) \rightarrow (10)$$

or, $t_2 = 0.405$ RC

$\rightarrow$ So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is,

$t_{HIGH} = t_1 - t_2$

$\quad t_{HIGH} = 1.09$ RC $- 0.405$ RC $= 0.69$RC

$\rightarrow$ So, for the given circuit,

$\quad t_{HIGH} = 0.69 (R_A + R_B)$ C $\rightarrow (11)$

$\rightarrow$ The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by,
$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}(1 - e^{-t/RC})$$

Solving, we get $t = 0.69$ RC

$\rightarrow$ So, for the given circuit,

$\quad t_{LOW} = 0.69$ RC $\rightarrow (12)$

$\rightarrow$ Here, both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, the total time is given by,

$T = t_{HIGH} + t_{LOW}$

or $T = 0.69 (R_A + 2R_B)$ C

So,

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \rightarrow (13)$$

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→ Fig. 18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency.

→ The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$.
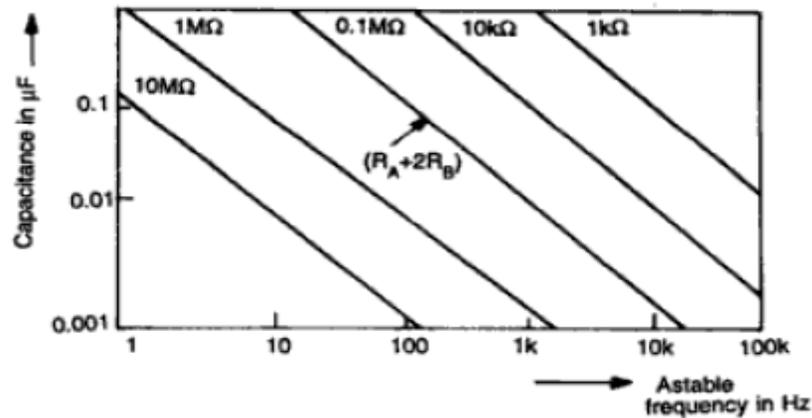
Figure 18: Frequency dependence of R_A, R_B and C

→ In this circuit, when the transistor Q_1 is ON, the output goes low. Hence,

$$\% D = \frac{t_{LOW}}{T} \times 100$$

$$\% D = \frac{R_B}{R_A + 2R_B} \times 100 \qquad \rightarrow(14)$$

→ With the circuit configuration of Fig. 15, it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69 (R_A + R_B)$ C will always be greater than $t_{LOW} = 0.69 R_B C$.

→ In order to obtain a symmetrical square wave i.e. D = 50%, the resistance R_A must be reduced to zero.

→ However, now pin 7 is connected directly to V_{CC} and extra current will flow through Q_1 when it is on.

→ This may damage Q_1 and hence the timer.

→ An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 19.

→ During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that,
$t_{HIGH} = 0.69 R_A C$
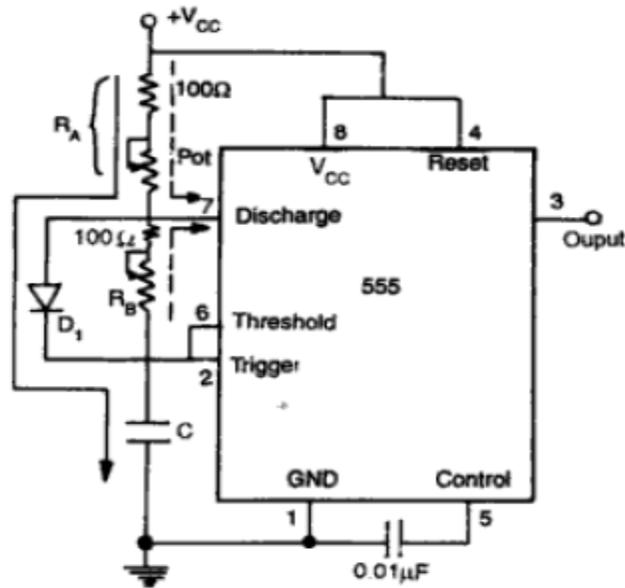
Figure 19: Adjustable duty cycle rectangular wave generator

→ However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

　　So,　　　　　　　　　　　　　$t_{LOW} = 0.69\, R_B C$　　　→ (15)

$T = t_{HIGH} + t_{LOW} = 0.69\, (R_A + R_B)\, C$　　→ (16)

Or,

$$f = \frac{1}{T} = \frac{1.45}{(R_A + R_B)C} \rightarrow (17)$$

And Duty Cycle is,

$$D = \frac{R_B}{R_A + R_B}$$

→ Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width.

→ However, a series resistor of 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value.

→ And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

→ Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the non-symmetrical square wave generator is shown in Fig. 20.

→ The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer.

→ The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

15
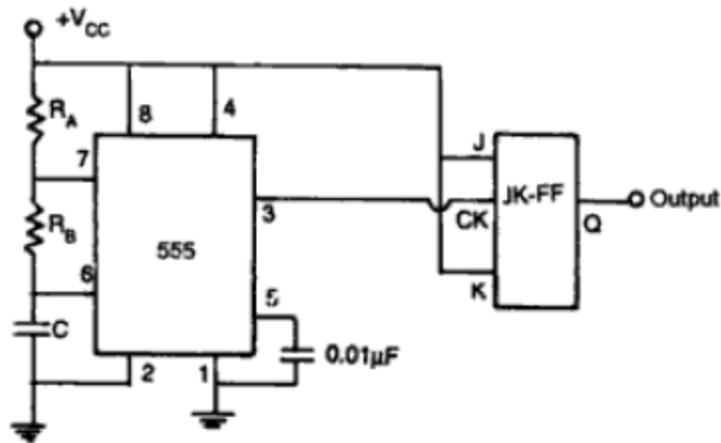
Figure 20: Symmetrical waveform generator

5. **Design an astable multivibrator that can produce an output with $T_{on}= T_{off}= 1$ msec. The OP-AMP is driven with a +15 and -15 V supply. Draw the waveforms across capacitors, feedback and output. The hysteresis should not exceed 0.1V. Nov/Dec 2019.**

Given Data:

$T_{on}= T_{off} = 1$ msec

$C= 0.01$ µF

$T= T_{on} + T_{off}$

$T= 2$ msec

$\quad D= T_{on}/ (T_{on} + T_{off})$

$\quad = (1$ msec$/ 2$ msec$) = 0.5$

$RA= (4/3)RB$

The period of oscillation $T= 0.693(RA + 2RB) \times C1$

$\qquad T= 0.693 \times (10/3\ RB) \times 10^{-8}$

$\qquad RB= 2$ms $\times (3/10) \times (1/ 0.693 \times 10^{-8})$

$\qquad RB= 86.5$ KΩ

$\qquad RA= (4/3) \times RB$

$\qquad = 115$ KΩ

16
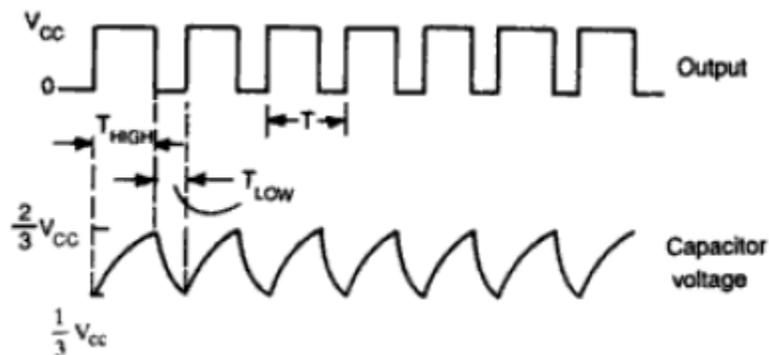
4.2.4   Applications in an Astable Mode:

> **6. Discuss some of the applications of Astable mode in detail?**

4.2.4.1 FSK Generator

→ In digital data communication, binary code is transmitted by shifting a carrier frequency between two pre-set frequencies.

→ This type of transmission is called frequency shift keying (FSK) technique.

→ A 555 timer in an Astable mode can be used to generate FSK signal.

→ The circuit is as shown in Fig. 21. The standard digital data input frequency is 150 Hz.

→ When input is HIGH, transistor Q is **off** and 555 timer works in the normal Astable mode of operation.

→ The frequency of the output waveform given by equation (1) can be rewritten as,

$$f_0 = \frac{1.45}{(R_A + 2R_B)C} \rightarrow (18)$$

→ In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals.

→ The components R_A and R_B and the capacitor C can be selected so that f_0 is 1070 Hz.
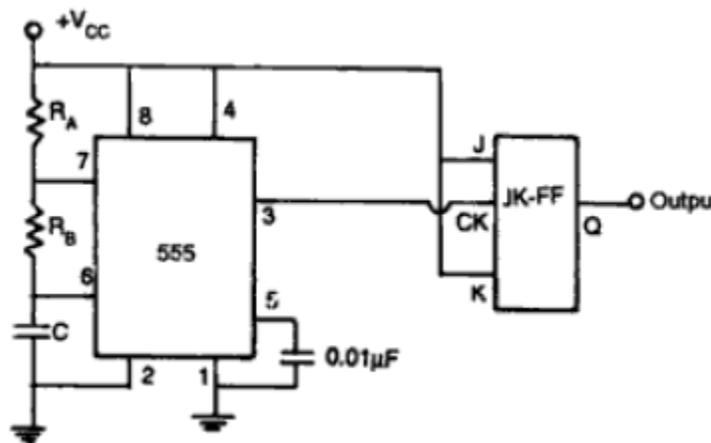
Figure 21 FSK generator

→ When the input is LOW, Q goes **on** and connects the resistance R_C across R_A. The output frequency is now given by,

$$f_0 = \frac{1.45}{(R_A \| R_C) + 2R_B} \rightarrow (19)$$

→ The resistance R_C can be adjusted to get an output frequency of 1270 Hz.

4.2.4.2 Pulse Position Modulator

→ The pulse position modulator can be constructed by applying a modulating signal to pin 5 of 555 timer connected for an Astable operation as shown in Fig. 22.
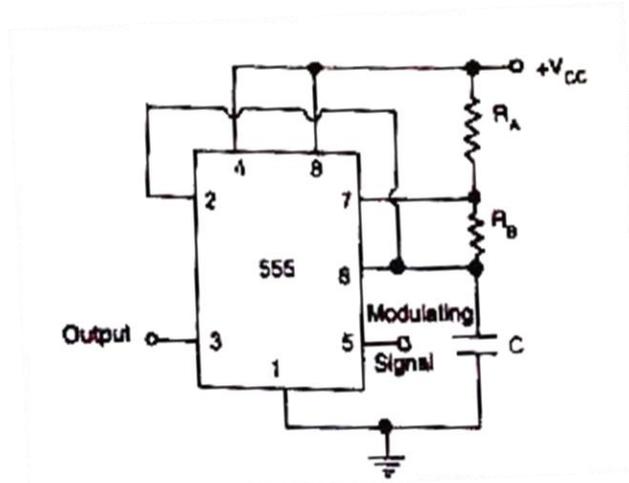
Figure 22: Pulse position modulator
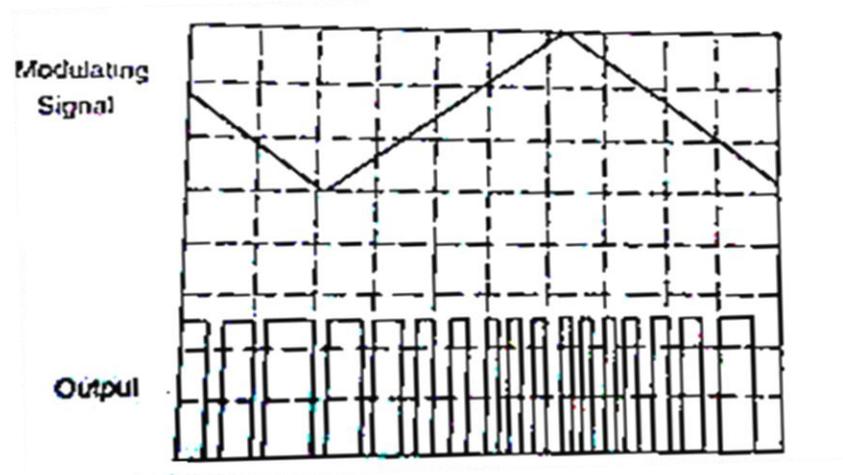
Figure 23: Pulse position modulator output

$\rightarrow$ The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

$\rightarrow$ Fig. 23 shows the output waveform generated for a triangle wave modulation signal.

$\rightarrow$ It may be noted from the output waveform that the frequency is varying leading to pulse position modulation.

$\rightarrow$ The typical practical component values may be noted as,

R_A=3.9kΩ R_B=3kΩ C= 0.01 μF

V_{CC} = 5V (any value between 5V to 18V may be chosen)

4.2.4.3 Schmitt Trigger

5   Write short notes on Schmitt Trigger.

$\rightarrow$ The use of a 555 timer as a Schmitt Trigger is shown in Fig. 24.

$\rightarrow$ Here the two internal comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2.

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$\rightarrow$ Since the upper comparator will trip at $(2/3)\ V_{CC}$ and lower comparator at $(1/3)\ V_{CC}$, the bias provided by R_1 and R_2 is centered within these two thresholds.
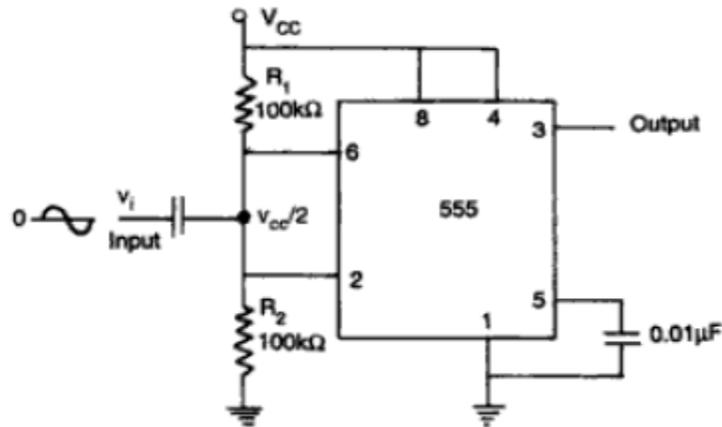
Figure 24: Timer in Schmitt trigger operation

$\rightarrow$ Thus, a sine wave of sufficient amplitude ($> V_{CC}/6 = 2/3\ V_{CC} - V_{CC}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 25.
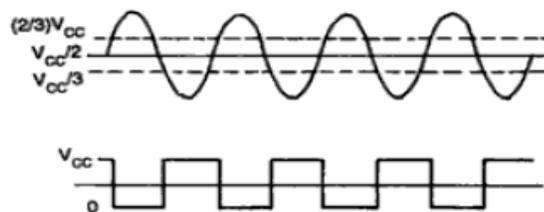
Figure 25: Input Output waveforms of Schmitt Trigger

$\rightarrow$ It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

4.3 566 VOLTAGE CONTROLLED OSCILLATOR IC

5 Give the block diagram of IC 566 VCO and explain its operation.[Nov/Dec 2012][April/May 2011][Nov/Dec 2010][Nov/Dec 2016].

(or)

6 Discuss the ICC 566 as a voltage controlled oscillator with necessary illustrations. [Apr/May 2019].

4.3.1 Voltage Controlled Oscillator (VCO):

$\rightarrow$ A common type of VCO available in IC form is Signetics NE/SE566.The pin configuration and basic block diagram of 566 VCO are shown in Fig. 26 (a, b).

$\rightarrow$ Referring to Fig. 26 (b), a timing capacitor C, is linearly charged or discharged by a constant current source/sink.

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→ The amount of current can be controlled by changing the voltage v_C applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip.

→ The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

→ The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1.

→ The output voltage swing of the Schmitt trigger is designed to V_{CC} and $0.5\ V_{CC}$.

→ If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from $0.5\ V_{CC}$ to $0.25\ V_{CC}$.

→ In Fig. 26 (c), when the voltage on the capacitor C_T exceeds $0.5\ V_{CC}$ during charging, the output of the Schmitt trigger goes LOW ($0.5\ V_{CC}$).

→ The capacitor now discharges and when it is at $0.25\ V_{CC}$, the output of Schmitt trigger goes HIGH (V_{CC}).
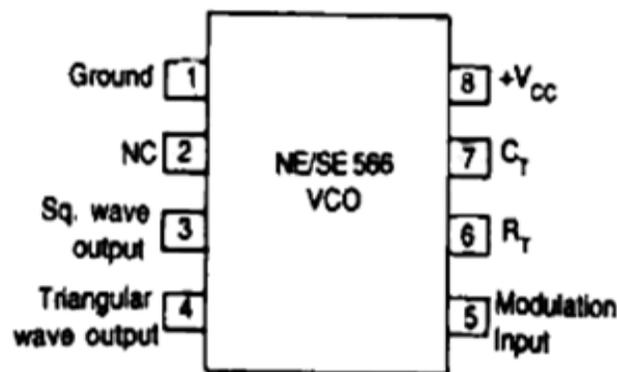
Figure 26 (a) Pin configuration
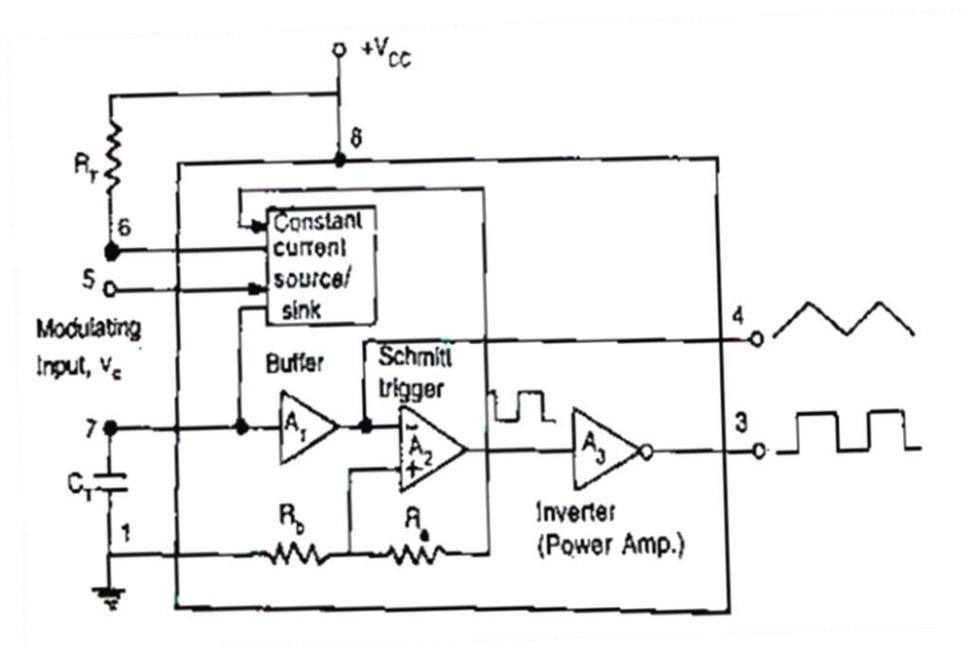
Figure 26(b): Block diagram

→ Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.

→ This gives a triangular voltage waveform across C_T which is also available at pin 4.

→ The square wave output of the Schmitt trigger is inverted by inverter A_3 and is available at pin 3.

→ The output waveforms are shown in Fig. 26 (c). The output frequency of the VCO can be calculated as follows:

→ The total voltage on the capacitor changes from 0.25 V_{CC} to 0.5 V_{CC}. Thus $\Delta v = 0.25$ V_{CC}. The capacitor charges with a constant current source.

So,

$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

Or,

$$\frac{0.25 V_{CC}}{\Delta t} = \frac{i}{C_T}$$

Or,

$$\Delta t = \frac{0.25 V_{CC} C_T}{i} \rightarrow 1$$

→ The time period T of the triangular waveform = 2Δt. The frequency of oscillator f_0 is,

$$f_0 = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{CC} C_T}$$

But,

$$i = \frac{V_{CC} - v_C}{R_T} \rightarrow 2$$

Where, v_C is the voltage at pin 5. Therefore,

$$f_0 = \frac{2(V_{CC} - v_C)}{V_{CC} C_T R_T} \rightarrow 3$$
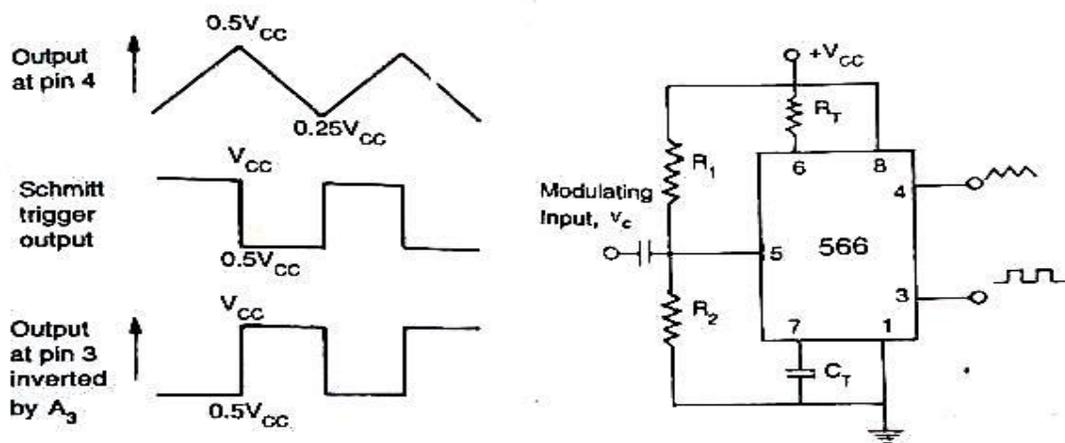
Figure 26(c): Output waveform   (d): Typical connection diagram

→ The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T, or (iii) the voltage v_C at the modulating input terminal pin 5.

→ The voltage v_C can be varied by connecting a R_1R_2 circuit as shown in Fig.26 (d).

→ The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range.

→ Now the modulating input voltage is usually varied from 0.75 V_{CC} to V_{CC} which can produce a frequency variation of about 10 to 1.

→ With no modulating input signal, if the voltage at pin 5 is biased at (7/8) V_{CC}, Eq. (9 10) gives the VCO output frequency as,

$$f_0 = \frac{2(V_{CC} - (7/8)V_{CC})}{V_{CC}C_TR_T} = \frac{1}{4C_TR_T} = \frac{0.25}{C_TR_T} \rightarrow 4$$

4.3.2 Voltage to Frequency Conversion Factor:

→ A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as,

$$K_v = \frac{\Delta f_0}{\Delta v_C}$$

→ Here Δv_C is the modulation voltage required to produce the frequency shift Δf_0 for a VCO.

→ If we assume that the original frequency is f_0 and the new frequency is f_1 then,

$$\Delta f_0 = f_1 - f_0 = \frac{2(V_{CC} - v_C + \Delta v_C)}{V_{CC}C_TR_T} - \frac{2(V_{CC} - v_C)}{V_{CC}C_TR_T}$$

$$\Delta f_0 = \frac{2\Delta v_C}{V_{CC}C_TR_T} \rightarrow 5$$

Or,

$$\Delta v_C = \frac{\Delta f_0 V_{CC}C_TR_T}{2} \rightarrow 6$$

Putting the value of C_TR_T from equation ()

$$\Delta v_C = \Delta f_0 V_{CC}/8f_0 \rightarrow 7$$

Or,

$$K_v = \frac{\Delta f_0}{\Delta v_C} = \frac{8f_0}{V_{CC}} \rightarrow 8$$

22

> **7   Explain the principle and operation of a PLL. [Nov/Dec 2013]**
>
> <center>(or)</center>
>
> **Explain the working of IC 565. [Nov/Dec 2013][April/May 2010][April/May 2011][April/May 2017][Nov/Dec 2015]**
>
> <center>(or)</center>
>
> **Explain with neat diagram, the working of a phase locked loop. Nov/Dec 2019.**

4.4.1 MONOLITHIC PHASE-LOCKED LOOP:

$\rightarrow$ All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL.

$\rightarrow$ However, a number of manufacturers have introduced monolithic PLLs too.

$\rightarrow$ Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor.

$\rightarrow$ The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges.

$\rightarrow$ Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

4.4.2 IC PLL 565:

$\rightarrow$ 565 are available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 27 (a, b).

$\rightarrow$ The output frequency of the VCO (both inputs 2, 3 grounded) as given by equation () can be rewritten as,

$$f_0 = \frac{0.25}{C_T R_T} Hz \qquad\qquad \rightarrow 1$$

Where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9.

$\rightarrow$ A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range.

$\rightarrow$ It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input.

$\rightarrow$ A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_0 with input signal f_S.

$\rightarrow$ A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.
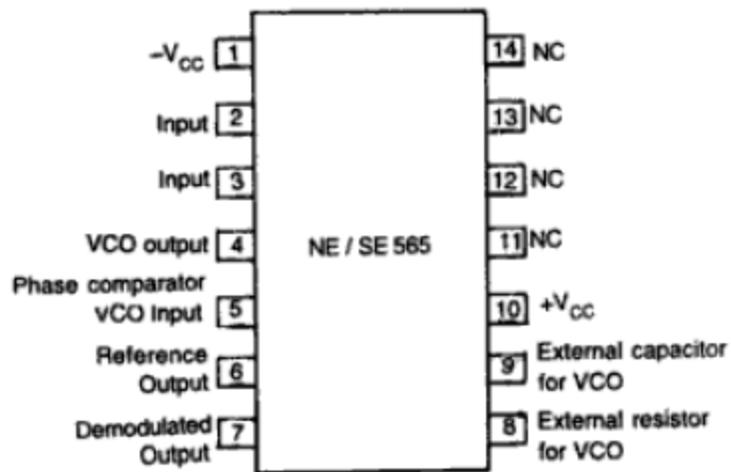
Figure 27(a): Pin Diagram
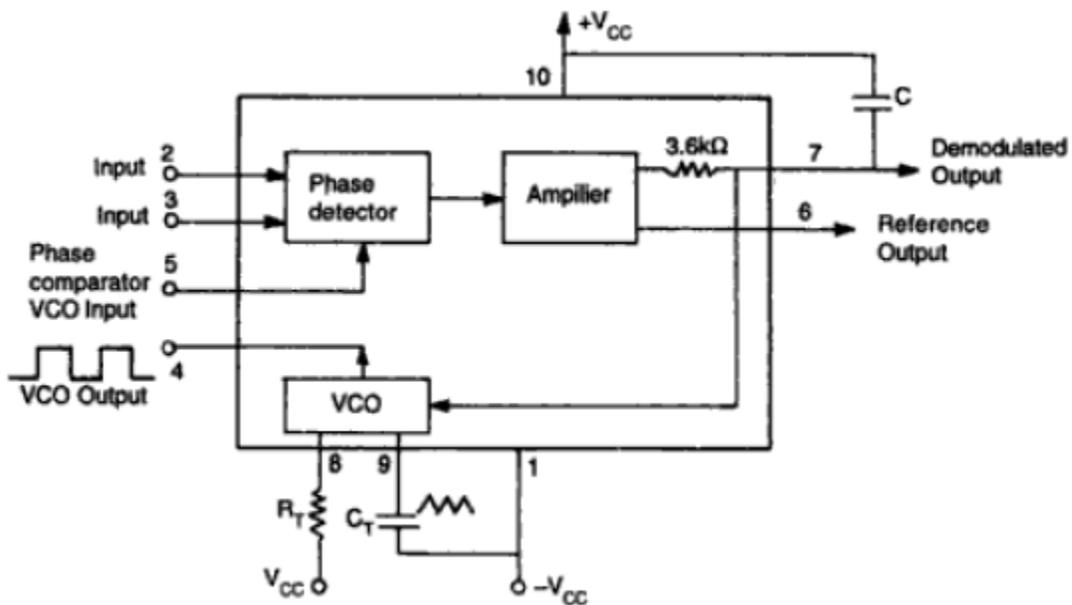
Figure 27 (b) NE/SE565 PLL block diagram

→ The important electrical parameters of 565 PLL are:

Operating frequency range : 0.001 Hz to 500 kHz

Operating voltage range : ±6V to ±12V

Input level : 10 mV rms min. to $3V_{PP}$ max

Input impedance : 10 kΩ typical

Outputs sink current : 1 mA typical

Drift in VCO centre frequency: 300 ppm/°C (parts per million per degree with Temperature centigrade)

Drift in VCO centre frequency: 1.5 percent / Vmax With supply voltage

24

<table>
<tr><td>Triangle wave amplitude</td><td>:</td><td>2.4 V_{pp} at $\pm$ 6 V supply voltage</td></tr>
<tr><td>Square wave amplitude</td><td>:</td><td>5.4V_{pp} at $\pm$ 6 V supply voltage</td></tr>
<tr><td>Bandwidth adjustment range:</td><td></td><td>$<\pm$ 1 to$\pm60\%$</td></tr>
</table>

$\rightarrow$ The capture range is symmetrically located with respect to VCO free running frequency f_0 as is shown in Fig. 28.

$\rightarrow$ The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range.

$\rightarrow$ In order to increase the ability of lock-in range, large capture range is required.

$\rightarrow$ However, a large capture range will make the PLL more susceptible to noise and undesirable signal.

$\rightarrow$ Hence a suitable compromise is often reached between these two opposing requirements of the capture range.

$\rightarrow$ Many a times the LPF band-width is first set for a large value for initial acquisition of signal, then once the signal is captured, the band-width of LPF is reduced substantially. This will minimize the interference of undesirable signals and noise.

---

8 **With Usual notations, show that the 'lock-in-range' of PLL is $\Delta f_L = \pm 7.8 f_0$ / V. [Nov/Dec 2011].**

$\rightarrow$ If φ radians are the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$v_e = (\varphi - \pi/2)$ ------------------- (1)

Wh, is the phase angle-to-voltage transfer coefficient of the phase detector.

$\rightarrow$ The control voltage to VCO is,

$v_c = (\varphi - \pi/2)$ ------------------ (2)

Where, A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$f = f_0 + K_v v_c$ ------------------- (3)

Where, K_v is the voltage to frequency transfer coefficient of the VCO.
When PLL is locked-in to signal frequency f_s, then we have

$f = f_s = f_0 + K_v v_c$ ------------------ (4)

Since, $v_c = (f_s - f_0) / K_v = AK_\varphi(\varphi - \pi/2)$ ------------------ (5)

Thus, $\varphi = \pi/2 + (f_s - f_0)/K_V K_\varphi A$ ------------------- (6)

$\rightarrow$ The maximum output voltage magnitude available from the phase detector occurs for $\varphi = \pi$ and 0 radian and $v_e(\max) = \pm K_\varphi . \pi/2$ The corresponding value of the maximum control voltage available to drive the VCO will be,

$v_{c(\max)} = \pm \left(\frac{\pi}{2}\right). K_\varphi . A$ -------------------- (7)

→ The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_0)_{max} = K_v V_{c(max)} = K_V K_\varphi A\left(\frac{\pi}{2}\right)$$ ------------------- (8)

→ Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_0 \pm (f - f_0)_{max}$$

$$= f_0 \pm K_V K_\varphi A\left(\frac{\pi}{2}\right) = f_0 \pm \Delta f_L$$ ------------------- (9)

Where $2\Delta f_L$ will be lock-in frequency range and is given by,

Lock-in range $= 2\Delta f_L = K_V K_\varphi A\pi$ ------------------- (10)

$$\Delta f_L = \pm K_V K_\varphi A\left(\frac{\pi}{2}\right)$$ ------------------- (11)

→ The lock in range is symmetrically located with respect to VCO free running frequency f_0. For IC PLL 565,

$$K_V = \frac{8f_0}{V}$$

Where, $V = +V_{cc} - (-V_{cc})$

Again, $K_\varphi = \frac{1.4}{\pi}$

And $A = 1.4$

Hence the lock-in range from eqn (11) becomes,

$$\boxed{\Delta f_L = \pm 7.8 \, f_0 \, / \, V}$$ ---------------- (12)

---

9 **Derive the expression for the capture range of PLL.**

→ When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_0. The phase angle difference between the signal and the VCO output voltage will be,

$$\varphi = (\omega_s t + \theta_s) - (\omega_0 t + \theta_0) = (\omega_s - \omega_0)t + \Delta\theta$$ ---------------- (13)

→ Thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\varphi}{dt} = \omega_s - \omega_0$$ ---------------- (14)

→ The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\varphi\left(\frac{\pi}{2}\right)$ and a fundamental frequency $(f - f_0) = \Delta f$.

→ The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) \approx \frac{1}{1 + j\left(\frac{f}{f_1}\right)}$$ ---------------- (15)

Where, $f1 = \frac{1}{2} \pi$ RC is the 3 dB point of LPF. In the slope portion of LPF where $(f/f1)^2 \gg 1$, then

$T(f) = \frac{f_1}{jf}$ ----------------- (16)

→ The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_0$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$T(\Delta f) \approx f_1/\Delta f = f_1/(f_s - f_0)$ ----------------- (17)

→ The voltage v_c to drive the VCO is,

$v_c = v_e \times T(f) \times A$ ----------------- (18)

Or, $v_{c(max)} = v_{e(max)} \times T(f) \times A$

$= \pm K_\varphi \left(\frac{\pi}{2}\right) A(f_1/\Delta f)$ [From eqn.7] ----------------- (19)

→ Then the corresponding value of the maximum VCO frequency shift is,

$(f - f_0)_{max} = K_V v_{c(max)} = \pm K_\varphi \left(\frac{\pi}{2}\right) A(f_1/\Delta f)$ ------------------ (20)

→ For the acquisition of signal frequency, we should put $f = f_s$ so that the maximum signal frequency range that can be acquired by PLL is,

$(f - f_0)_{max} = \pm K_V K_\varphi \left(\frac{\pi}{2}\right) A(f_1/\Delta f_c)$ ----------------- (21)

Now, $\Delta f_c = (f - f_0)_{max}$

So,

$(\Delta f_c)^2 = \pm K_V K_\varphi \left(\frac{\pi}{2}\right) A f_1$ [From eqn.21]

Since, $\Delta f_L = \pm K_V K_\varphi \left(\frac{\pi}{2}\right) A$

We get, $(\Delta f_c) = \pm \sqrt{f_1 \Delta f_L}$ ----------------- (22)

→ Therefore, the total capture range is,

$$2\Delta f_c \approx 2\sqrt{f_1 \Delta f_L}$$

Where the lock-in range $= 2\Delta f_c = K_V K_\varphi A\pi$. In case of IC PLL 565, R = 3.6 KΩ, so the capture range is

$\pm \left[\dfrac{\Delta f_L}{2\pi(3.6 \times 10^3)}\right]^{\frac{1}{2}}$ ----------------- (23)

Where, C is in farads.

→ The capture range is symmetrically located with respect to VCO free running frequency f_0 as shown in the figure below.

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→ The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range.

→ In order to increase the ability of lock-in range large capture range is required.

→ However, a large capture range will make the PLL more susceptible to noise and undesirable signal.

→ Hence a suitable compromise is often reached between these two opposing requirements of the capture range.

→ Many a times the LPF bandwidth is first set for a large value for initial acquisition of signal, then once the signal is captured, the bandwidth of LPF is reduced substantially.

→ This will minimize the interference of undesirable signals and noise.

Figure 28: PLL lock in range and capture range

PROBLEM:

10 Determine the output frequency f0, lock range Δfl and capture range Δfc of IC 565. Assume R1 = 15Ω, C1= 0.01µF and the supply voltage is +12V. (Apr/May 2019) 15 marks.

Output frequency (f_0)

$$f_0 = \frac{0.25}{C_T R_T} Hz$$

$= 0.25/ (0.01 \times 10^{-6} \times 15)$

$f_0 = 1.6$ MHz

lock range (Δf_L)

$f_L = \pm 7.8 \, f_0 / $ V

$f_L = 1.03$ MHz

capture range Δfc

$$\pm \left[\frac{\Delta f_L}{2\pi(3.6 \times 10^3)} \right]^{\frac{1}{2}}$$

$$\sqrt{\frac{[1.3 \times 10^6]}{2\,\pi \times 3.6 \times 10^3 \times 1 \times 10^{-6}}}$$

Δfc = 127.6MHz

4.4.3 PLL APPLICATIONS

11 Mention briefly the applications of PLL. [April/May 2008][Apr/May 2011][April/May 2013][Nov/Dec 2016]

$\rightarrow$ The output from a PLL system can be obtained either as the voltage 7 signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal.

$\rightarrow$ The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

$\rightarrow$ Consider the case of voltage output.

$\rightarrow$ When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to $(f_s\text{-}f_0)$.

$\rightarrow$ If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock.

$\rightarrow$ Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

$\rightarrow$ In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input.

$\rightarrow$ The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies.

$\rightarrow$ VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed now.

4.4.3.1 Frequency Multiplication/Division

$\rightarrow$ Figure 30 gives the block diagram of a frequency multiplier using PLL.

$\rightarrow$ A divide by N network 18 inserted between the VCO output and the phase comparator input.

$\rightarrow$ In the locked state, the VCO output frequency f_0 is given by,

$f_0 = N\ f_s \rightarrow 1$

$\rightarrow$ The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

$\rightarrow$ Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

$\rightarrow$ If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to then the harmonic of the input signal without connecting any frequency divider in between.
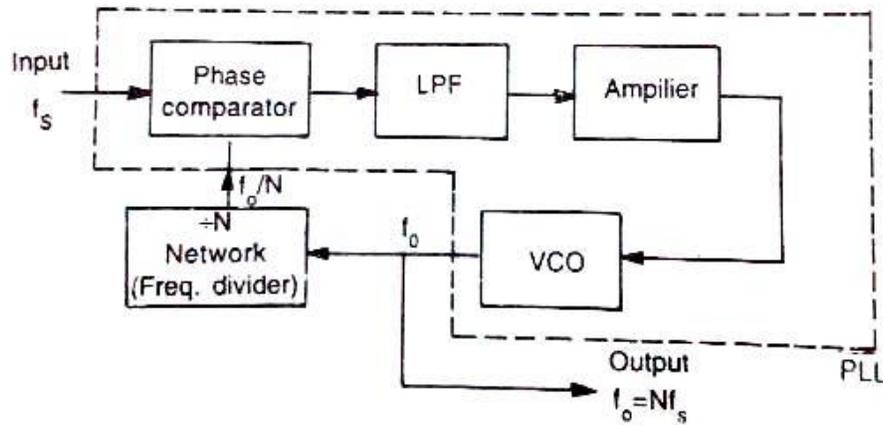
Figure 29: Frequency multiplier using IC PLL

→ However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of 12. Typically n is kept less than 10.

→ The circuit of Fig. 28 can also be used for frequency division.

→ Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_5.

→ The output f_0 of VCO is now given by

$$f_o = f_s/m \qquad\qquad →2$$

4.4.3.2 Frequency Translation

→ A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 31.

→ It can be seen that a mixer (or multiplier) and a low-pass filter are connected externally to the PLL.

→ The signal f_S which has to be shifted and the output frequency f_o of the VCO are applied as inputs to the mixer.

→ The output of the mixer contains the sum and difference of f_s and f_0.

→ However, the output of LPF contains only the difference signal $(f_o - f_s)$.

→ The translation or offset frequency $f_1(f_l<<f_s)$ is applied to the phase comparator.

Figure 30: PLL used as a frequency translator

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$\rightarrow$ When PLL is in locked state,

$$f_o - f_s = f_1$$
$$f_o = f_s + f_1 \rightarrow 3$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

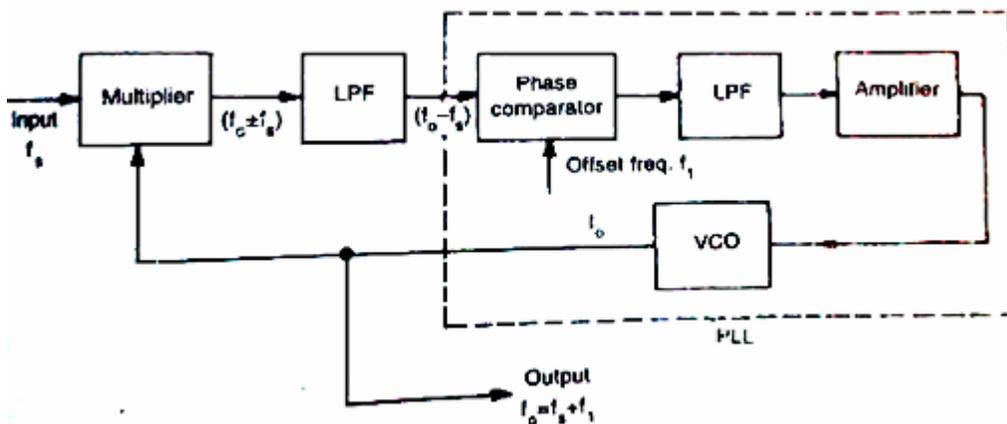### 4.4.3.3 AM Detection

$\rightarrow$ The PLL may be used to demodulate AM signals as shown in figure below. The PLL is locked to the carrier frequency of the incoming AM signal.

$\rightarrow$ The output of VCO which has the same frequency as the carrier, but un modulated is fed to the multiplier.

$\rightarrow$ Since VCO output is always 90^0 out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90^0 before being fed to the multiplier.

$\rightarrow$ This makes both the signals applied to the multiplier in same phase.

$\rightarrow$ The output of the multiplier contains both the sum and the difference signals; the demodulated output is obtained after filtering high frequency components by the LPF.

$\rightarrow$ Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.
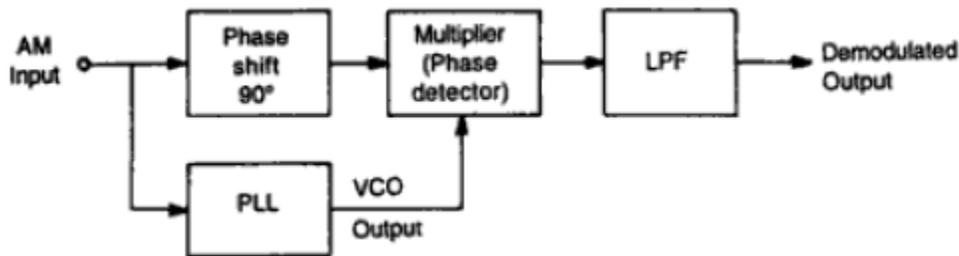
Figure 31: PLL used as AM demodulator

4.4.3.4 FM Demodulation

$\rightarrow$ If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.

$\rightarrow$ The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.

$\rightarrow$ The VCO transfer characteristics determine the linearity of the demodulated output.

$\rightarrow$ Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

4.4.3.5 Frequency Shift Keying (FSK) Demodulator

12   Narrate the process of FSK demodulation using PLL [Nov/Dec 2015] [May 2018] [6].

$\rightarrow$ In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies.

$\rightarrow$ This type of data transmission is called frequency shift keying (FSK) technique.

→ The binary data can be retrieved using a FSK demodulator at the receiving end.

→ The 565 PLL is very useful as a FSK demodulator.

→ Figure 30 shows FSK demodulator using PLL fortele - typewriter signals of 1070 Hz and 1270 Hz.

→ As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

→ A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.
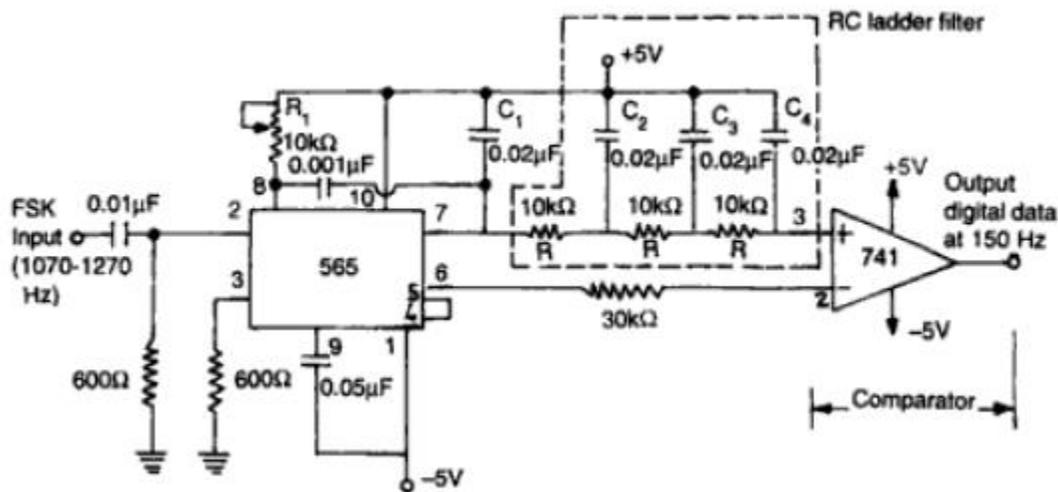
Figure 32: FSK Demodulator

4.5 ANALOG MULTIPLIER IC

13 **Discuss the modes of operation and applications of analog multiplier.**

→ A multiplier is a circuit which produces output that is the product of two inputs applied.

→ A circuit which performs multiplication of two analog voltages is called as analog multiplier.

→ If V_1 and V_2 were the two input analog voltages applied, then the output voltage V_0 is given as,

$V_0 = k\ V_1\ V_2$

Where, k – scaling factor

→ The use of a scaling factor k is to avoid the saturating output.

→ This is because; the product of two input voltages with moderate value could cause the output to reach saturation.

→ In such a situation, it may become impossible to measure the desired product output V_0.

→ The above expression for V_0 is the ideal output voltage. They are

    (i)   Input signal offset (φ_1 & φ_2)

    (ii)   Error in scaling factor k (e)

    (iii)   Output signal offset (φ_0)

→ With all these parameters, the output of a practical multiplier is given as V_0 defined by,

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$$V_0 = \frac{(V_1 + \varphi_1)(V_2 + \varphi_2)}{10^X(1 + e)} + \varphi_0$$

→ Note that x can be any integer or fractional value.

4.5.1 Modes of operation of a multiplier

→ The modes of operation of multiplier tell about the restriction on polarity of one or both input voltages V_1 and V_2 applied to multiplier. There were three modes

   ❖ One quadrant multiplication
   ❖ Two quadrant multiplication
   ❖ Four quadrant multiplication

One quadrant

→ Both input voltages V_1 and V_2 are restricted to positive polarity.

→ That is, V_1 and V_2 must be positive as shown here. It uses first quadrant.
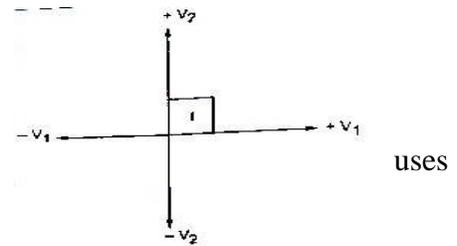
Figure 33(a): one quadrant

Two quadrant

→ In this mode, any one input voltage V_1 or V_2 is held positive and the other is allowed to swing in both positive and negative polarity.

→ It uses any two of four quadrants (Quadrant I and II or I and IV) as shown here.
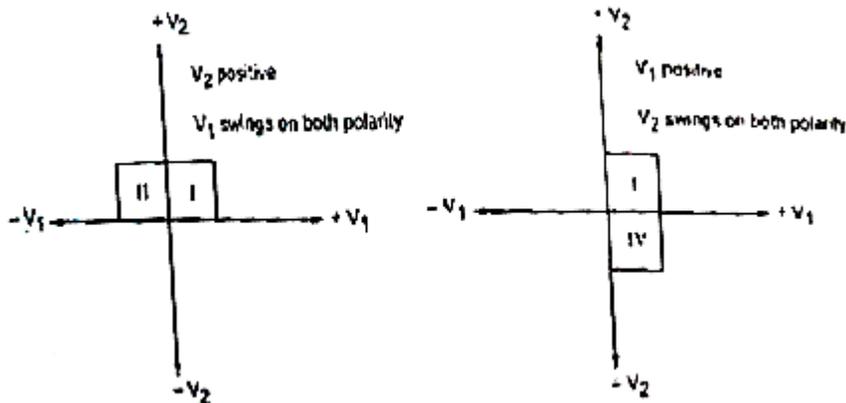
Figure 33(b): two quadrant

Four quadrant (Gilbert cell)

→ In this mode, both the input voltages V_1 and V_2 are allowed to swing in both positive and negative polarity.

→ It uses all four quadrants and hence the same. The figure here shows the four quadrant multiplication.

→ Also, it is clear that not only the input voltages are restricted in the modes; the output voltage V_0 is also restricted.

→ In one quadrant multiplication, the output voltage V0 must be positive since both inputs are positive.

→ But, in two quadrant and four quadrant multiplication, the output can be positive or negative depending on input voltage polarity.

→ Three quadrant operations is impossible in multiplier because no restriction can be made in input voltages.

→ Out of all modes of operation, four quadrants is best and popular.
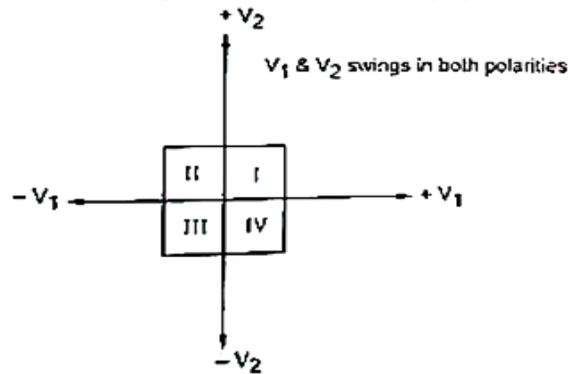
Figure 33(c): four quadrant

4.5.2 Types of Analog multipliers

❖ The basic techniques used to achieve multiplication are
❖ Logarithmic type
❖ Quarter square type
❖ Pulse width / height modulation type
❖ Current rating type
❖ Triangle averaging type
❖ Emitter coupled transistor pair type
❖ Variable Trans conductance type
❖ Four quadrant type based on variable Trans conductance (or) simply, Gilbert cell.

4.5.3 Characteristics (or) Requirements of a multiplier

→ The following characteristics or requirements are very important for a multiplier to achieve maximum efficiency. They are defined here,

Accuracy

→ The derivation of practical output from the ideal output of multiplier for the given input voltages within the operating range of multiplier.

→ This characteristic tells how accurate the multiplier is and whether the expected output is obtained or not.

Linearity

→ It is the maximum percentage deviation that a practical output compared with a linear straight line output (ideal output).

Squaring mode accuracy

→ The accuracy of multiplier when both inputs tied together gives square-law curve.

→ The deviation of practical squared output versus ideal square-law curve is squaring mode accuracy.

Bandwidth

→ The operating capability of an amplifier for high frequency analog inputs is indicated with bandwidth.

$\rightarrow$ Capability with as high frequency as possible indicates the improvement in bandwidth.

Quadrant

$\rightarrow$ Defines the unipolar or bipolar capabilities of input voltages applied.

14 **Explain the working of an analog multiplier using emitter coupled transistor pair. [Nov/Dec 2014][May/June 2014][Nov/Dec 2011]**

$\rightarrow$ A pair of transistor with their emitter connected together forms a basic multiplier.

$\rightarrow$ One input V1 can be directly applied to the base of transistors Q1 and Q2.

$\rightarrow$ The other input V2 is applied as the emitter current to both transistors as shown in figure below.
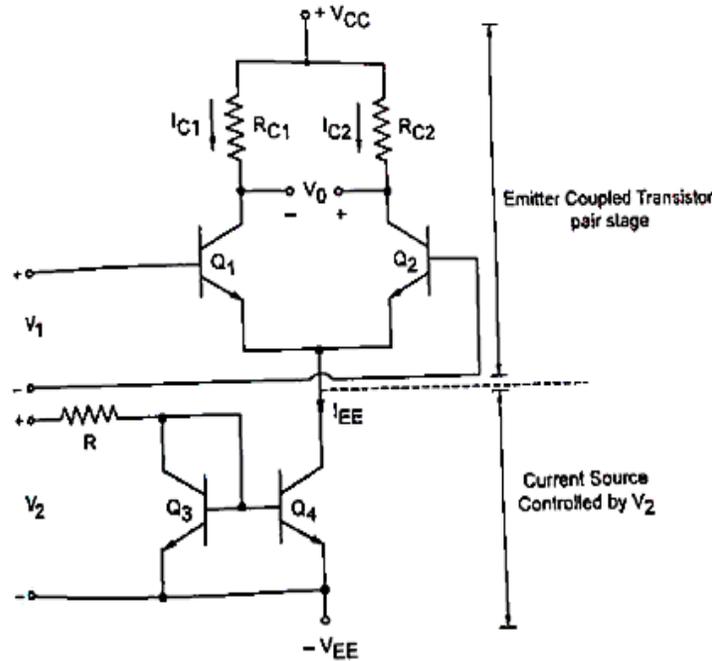
Figure 34: Emitter coupled transistor

$\rightarrow$ Taking only the emitter coupled transistor pair stage, the output currents (collector currents) I_{C1} and I_{C2} are related to the differential input voltage V_1 by

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_1/V_T}}$$

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_1/V_T}}$$

Where V_T is the temperature equivalent voltage and the polarity in exponential terms depends on the input voltage V_1.

$\rightarrow$ The polarity is negative when positive input of V_1 applied to base of transistor Q_1

$\rightarrow$ The polarity is positive when the negative input of V_1 applied to base of transistor Q_2.

$\rightarrow$ Taking the difference between two collector currents I_{C1} and I_{C2} as ΔI_C, we can write

$\Delta I_C = I_{C1} - I_{C2}$

Substituting the values of I_{C1} and I_{C2} in above expression

$$\Delta I_C = \frac{I_{EE}}{1 + e^{-V_1/V_T}} - \frac{I_{EE}}{1 + e^{V_1/V_T}}$$

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$$= I_{EE}\left[\frac{1}{1 + e^{-V_1/V_T}} - \frac{1}{1 + e^{V_1/V_T}}\right]$$

$$\Delta I_C = I_{EE}\tanh\left(\frac{V_1}{2V_T}\right) \qquad \text{-------------------- (1)}$$

→ The DC transfer characteristics of the emitter coupled pair are shown in figure below.

Figure 35: DC characteristics

→ If $V_1 \ll V_T$, eqn. (1) can be approximated as

$$\Delta I_C = I_{EE}\tanh\left(\frac{V_1}{2V_T}\right) \cong I_{EE}\left(\frac{V_1}{2V_T}\right) \qquad \text{-------------------- (2)}$$

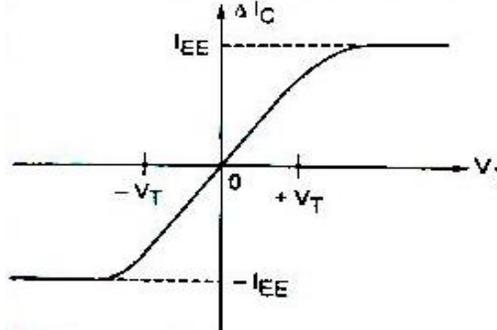→ I_{EE} is the bias current for emitter-coupled pair. If I_{EE} is made proportional to the second input V_2, then eqn. (2) becomes

$$\Delta I_C = V_2\left(\frac{V_1}{2V_T}\right) \text{ where } V_2 \; \alpha \; I_{EE}$$

→ Thus the collector difference current is proportional to the product of two input voltages V_1 and V_2 multiplied by factor $\frac{1}{2V_T}$. But, considering the base to emitter voltage of transistor, I_{EE} can be written as

$$I_{EE} \cong K_0\left(V_2 - V_{BE(ON)}\right) \qquad \text{-------------------- (3)}$$

Substitute the value of I_{EE} from eqn. (3) in ΔI_C of eqn. (2) we get

$$\Delta I_C = \frac{K_0 V_1\left(V_2 - V_{BE(ON)}\right)}{2V_r}$$

→ Where, k_0 is the scaling factor. Two conditions must be satisfied by the input voltages in order to perform multiplication. V_1 must be less than 50 mV and V_2 must be greater than $V_{BE(ON)}$.

4.5.4 Drawbacks

→ The input voltage V_2 is offset by $V_{BE(ON)}$. So the desired input V_2 cannot be multiplied with other input V_1. Thus the preciseness in getting the product output is affected.

→ V_2 must be always positive resulting in two-quadrant multiplication.

→ $\tanh\left(\frac{V_1}{2V_T}\right)$ is approximated as $\left(\frac{V_1}{2V_T}\right)$ with the assumption $V_1 \ll V_T$

→ In room temperature, $V_T = 26mV$. Therefore, V_1 must be very small to satisfy the approximation.

---

15 **Explain Gilbert multiplier cell. Under what condition the Gilbert multiplier cell will work as a modulator. [Nov/Dec 2009][Nov/Dec 2013]**

→ The first two drawbacks of emitter coupled transistor pair multiplier can be eliminated by Gilbert multiplier cell.
→ Gilbert multiplier cell is also known as four-quadrant multiplier cell.
→ It allows the two input voltages to swing in both polarities.
→ This method is an extension of emitter coupled transistor pair. The circuit of Gilbert cell is shown in figure below.
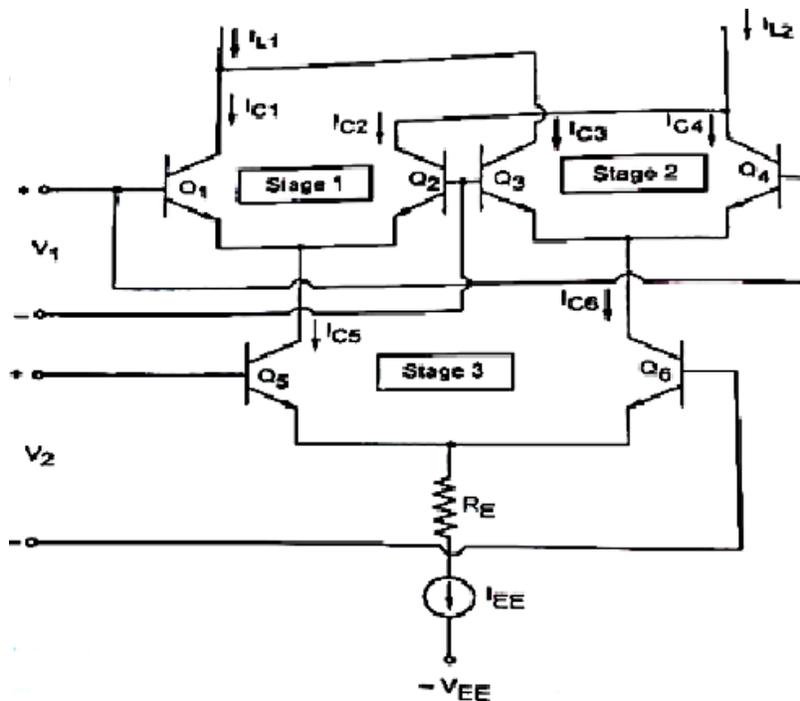
Figure 36: Gilbert multiplier cell

→ The circuit consists of three stages with each stage having a pair of transistors.
→ All the stages are emitter coupled transistor pair with cross coupled stages 1 and 2 in series with stage 3.
→ The analysis of the circuit can be done using two methods.
→ Analysis 1 uses hyperbolic tangent function and analysis 2 uses the basic principle of Tran's conductance dependence.

Analysis 1:

→ As related to discussion of emitter coupled transistor pair, the collector currents of all stages are related with input voltages as follows.
→ The collector current of Q_1 and Q_2 are given as,

$$I_{C1} = \frac{I_{C5}}{1+e^{-V_1/V_T}} \text{------------------ (1)}$$

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$$I_{C2} = \frac{I_{C5}}{1+e^{V_1/V_T}} \quad [\text{I}_{C5} \text{ is emitter current of pair Q}_1 \text{ and Q}_2]\text{------------------ (2)}$$

→ Similarly, collector currents of Q$_3$ and Q$_4$ are given as,

$$I_{C3} = \frac{I_{C6}}{1+e^{V_1/V_T}}\text{------------------ (3)}$$

$$I_{C3} = \frac{I_{C6}}{1+e^{-V_1/V_T}} \quad [\text{I}_{C6} \text{ is emitter current of pair Q}_3 \text{ and Q}_4] \quad \text{------------------ (4)}$$

→ And the collector current of Q$_5$ and Q$_6$ can be given as,

$$I_{C1} = \frac{I_{C5}}{1+e^{-V_1/V_T}}\text{------------------ (5)}$$

$$I_{C2} = \frac{I_{C5}}{1+e^{V_1/V_T}} \quad [\text{I}_{C5} \text{ is emitter current of pair Q}_1 \text{ and Q}_2] \quad \text{------------------ (6)}$$

→ Substituting the values of I$_{C5}$ and I$_{C6}$ from eqns. (5) and (6) in equations (1), (2), (3) and (4), we get,

$$I_{C1} = \frac{I_{EE}}{[1+e^{-V_1/V_T}][1+e^{-V_2/V_T}]}\text{------------------ (7)}$$

$$I_{C2} = \frac{I_{EE}}{[1+e^{V_1/V_T}][1+e^{-V_2/V_T}]}\text{------------------ (8)}$$

$$I_{C3} = \frac{I_{EE}}{[1+e^{V_1/V_T}][1+e^{V_2/V_T}]}\text{------------------ (9)}$$

$$I_{C4} = \frac{I_{EE}}{[1+e^{-V_1/V_T}][1+e^{V_2/V_T}]}\text{------------------ (10)}$$

→ The differential output current ΔI is given as,

$$\Delta I = I_{L1} - I_{L2}$$

Where, I$_{L1}$ = I$_{C1}$ + I$_{C3}$ and I$_{L2}$ = I$_{C2}$ + I$_{C4}$ from the figure

$$\therefore \Delta I = (I_{C1} + I_{C3}) - (I_{C2} + I_{C4})$$

$$[\text{or}]$$

$$\Delta I = (I_{C1} + I_{C4}) - (I_{C2} + I_3)\text{------------------ (11)}$$

→ Substitute the equation (7) to (10) in (11) and taking exponential terms as hyperbolic tangent functions, we get

$$\therefore \Delta I = I_{EE}\left[tanh\left(\frac{V_1}{2V_T}\right)tanh\left(\frac{V_2}{2V_T}\right)\right]$$

→ Thus the differential output ΔI is the product of the hyperbolic tangent of two input voltages V$_1$ and V$_2$.

→ The output voltage V_0 can be obtained from ΔI by using two equal value resistors R connected to V_{CC} and sending current $I_{L1} = (I_{C1} + I_{C3})$ through one resistor and $I_{L2} = (I_{C2} + I_{C4})$ through other resistor.

Analysis 2

→ The emitter currents of stage 1 and 2 are the collector currents of stage 3 (I_{C5} and I_{C6} in the figure).

→ The current relationships are

$$I_{C1} + I_{C2} = I_{C5}$$

$$I_{C3} + I_{C4} = I_{C6}$$

$$I_{C5} + I_{C6} = I_{EE}$$

→ Assume that $|V_1| and |V_2| \ll V_T$ and current imbalance is given by

$I_{C1} - I_{C2} = (g_m)_{12}V_1$ ----------------------- (1)

$I_{C3} - I_{C4} = (g_m)_{34}V_1$ ----------------------- (2)

Where, $(g_m)_{12}$ and $(g_m)_{34}$ are Trans conductance of pairs $Q_1 - Q_2$ & $Q_3 - Q_4$ respectively.

$$(g_m)_{12} = \frac{I_{C5}}{V_T}$$

$$(g_m)_{34} = \frac{I_{C6}}{V_T}$$

[In general, $g_m = \frac{I_E}{V_T}$ in Transconductance technique]

→ Here, I_{C5} and I_{C6} are nothing but emitter currents of stage 1 and stage 2 respectively. The differential output voltage V_0 is

$V_0 = R_L [(I_{C1} - I_{C2}) - (I_{C3} - I_{C4})]$ ------------------------ (3)

Substitute the equations (1) and (2) in (3), we get

$$V_0 = R_L[(g_m)_{12}V_1 - (g_m)_{34}V_1]$$

$$V_0 = R_L V_1 \left[\frac{I_{C5}}{V_T} - \frac{I_{C6}}{V_T}\right]$$

$$V_0 = \frac{R_L V_1}{V_T}(I_{C5} - I_{C6})$$ ----------------------- (4)

If R_E is chosen such that
$I_{C5} R_E \gg V_T$ & $I_{C6} R_E \gg V_T$ then,

$I_{C5} - I_{C6} = \frac{V_2}{R_E}$ ----------------------- (5)

Substitute eqn. (5) in (4)

$$V_0 = \frac{R_L V_1}{V_T}\left(\frac{V_2}{R_E}\right)$$

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Rearranging we get

$$V_0 = (V_1 V_2)\frac{R_L}{V_T R_E}$$

$V_0 = KV_1V_2$

Where $K = \frac{R_L}{V_T R_E}$ is the scaling factor.

$\rightarrow$ Thus the output voltage V_0 is the product of two input voltages V_1 and V_2 multiplied by scaling factor k.

Applications

❖ Used in most of the IC multipliers as a four quadrant cell.
❖ Used as modulators or mixers in communication circuits
❖ Used in signal processors.
❖ Used as detectors or demodulators to recover low frequency signals
❖ Used as phase detectors.
❖ Used as frequency doubler, squarer, square rooter, divider, etc.

17. with a neat diagram, explain the variable Trans conductance technique in analog multiplier and give its output equation. [April/May 2010][May/June 2009, 2018] [13].

$\rightarrow$ The following figure shows the differential stage used for variable Transconductance technique.

$\rightarrow$ The principle of operation is the dependence of transistor Transconductance on the emitter current bias applied.

$\rightarrow$ The emitter current bias is controlled by the second input voltage V_2. Q_1 and Q_2 in the circuit form the differential amplifier.

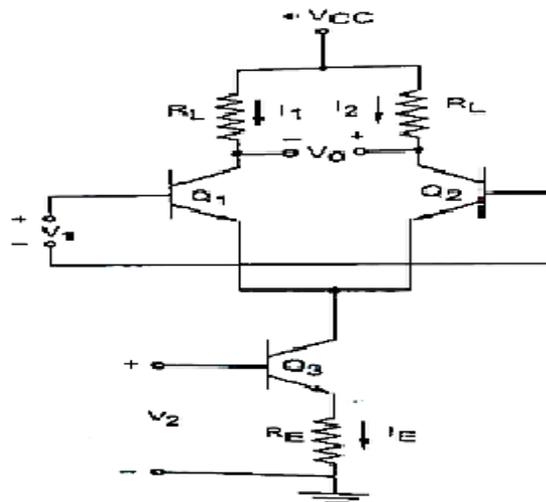**Figure 37: Variable trans conductance amplifier**

$\rightarrow$ For very small differential voltage $V_1 << V_T$ the output voltage is given as

$V_0 = g_m R_L V_1$ -------------------- (1)

Where, $g_m = \frac{I_E}{V_T}$ is the Trans conductance   ------------------ (2)

→ Note that V_0 depends on g_m and g_m depends on I_E. By changing V_2, I_E changes, thereby g_m changes. From the diagram,

$$V_2 = I_E R_E + V_{BE3}$$

→ If $I_E R_E >> V_{BE3}$

$$V_2 = I_E R_E \&$$

$$\text{Thus } I_E = \frac{V_2}{R_E}$$

Substitute I_E in (2) and then g_m in (1) we get

$$V_0 = \frac{V_2}{R_E V_T}. R_L V_1 \text{-------------------- (3)}$$

Rearranging (3), we get

$$V_0 = (V_1 . V_2) \frac{R_L}{R_E V_T}$$

$$\text{Take } K = \frac{R_L}{R_E V_T}$$

$V_0 = k\, V_1 . V_2$
& 'k' is the scaling factor.

→ To improve linearity of the multiplier, exponential current voltage characteristics can be converted to linear characteristics as shown in the following figure.
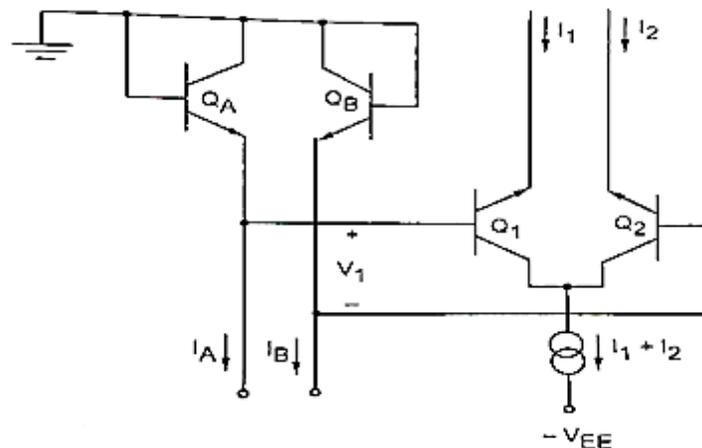

Figure 38: Improved linearity of multiplier

→ The two transistors Q_A & Q_B is a diode connected transistor and are driven by I_A & I_B, I_1 & I_2 are related as

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$$\frac{I_1}{I_2} = e^{(V_1/V_2)} \qquad\qquad \text{------------------- (4)}$$

And the net bias voltage V1 is logarithmic and given as

$$V_1 = V_T \ln\left(\frac{I_B}{I_A}\right)$$

And substituting V_1 in I_1/I_2 we get

$\frac{I_1}{I_2} = \frac{I_B}{I_A}$; Assuming that V_T is very small.

A four quadrant multiplier – complete circuit

→ As shown in figure, the complete circuit consists of voltage to current converters or current to voltage converters.

→ The currents I_9 and I_{10} through the emitters of Q_7 and Q_8 generate a voltage between two emitter terminals that is proportional to inverse hyperbolic tangent of V_1.

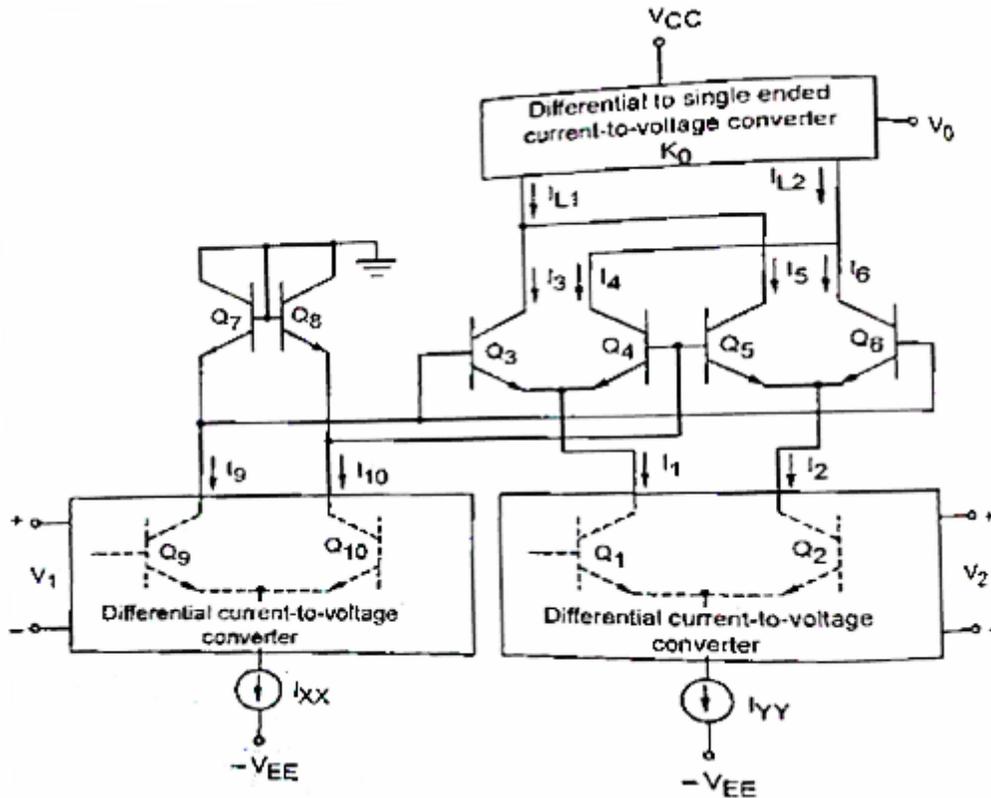→ It uses Gilbert cell for four quadrant multiplication.

Figure 39: four quadrant multiplication using Gilbert multiplier

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18. Write short notes on Analog multiplier ICs (Monolithic multipliers).

There were several multiplier Ics available. Important Ics are AD 533, AD 534 & AD 633.

4.6.1 AD 533

→ Accepts input upto 1 MHZ with 1% error.

4.6.2 AD 534

→ Provides maximum gain with error of ±0.25%.

→ Also provides excellent stability upto 10 KHz and a flexible IC.

4.6.3AD 633

→ This is a four quadrant analog multiplier.

→ It has high input impedance, operates with voltage ranging from ±8V to ±18V.

→ This IC needs no external components and calibration.

→ The range of the two input signals is ±10 V.

→ The pin diagram of AD 633 is shown in figure (b) and basic symbol of multiplier is shown in figure (a).

4.6.4 Symbol of a multiplier
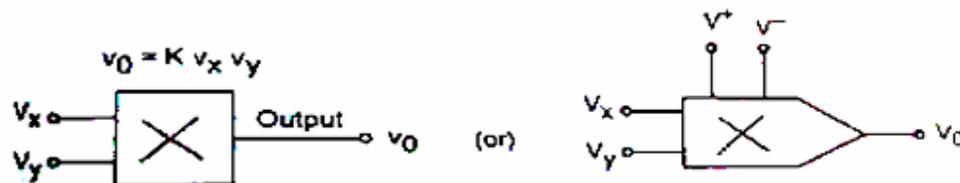
Figure 40(a): symbol for multiplier

→ The output voltage $V_0 = k\, V_x V_y$ where k is selected as $K = \dfrac{1}{V_{ref}} = \dfrac{1}{10V}$.

→ The reference voltage V_{ref} is internally set to 10 V.

→ The operating input voltage as can be $V_x = V_y \leq 10V$ until then the multiplier do not saturate.

→ The transfer characteristics of a four quadrant multiplier is shown in fig (b)

→ The above characteristics diagram shows the output voltage for both positive and negative input voltages.

→ The output voltage is positive when both inputs V_x and V_y are positive (or) negative.

→ The output is negative if any one input is (V_x or V_y) is negative.

→ The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node.
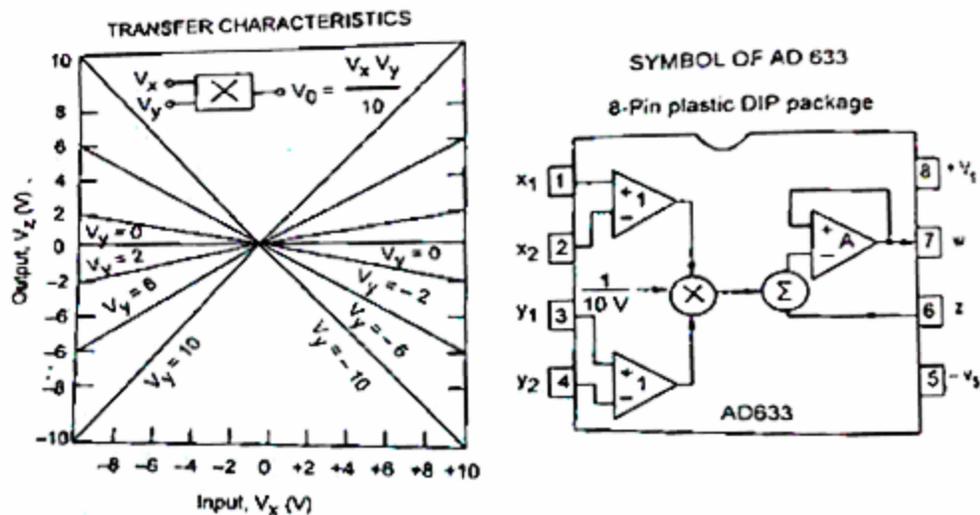
Fig 40(b) Transfer characteristics

→ The differential X and Y inputs are converted to differential currents by voltage-to-current converters.

→ The product of these currents is generated by the multiplying core.

→ A buried Zener reference provides an overall scale factor of 10 V. The sum of $(X \times Y)/10 + Z$ are then applied to the output amplifier.

→ The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computation functions.

4.6.5 APPLICATIONS

The AD633 is well suited for such applications as,

- ➢ Modulation
- ➢ Demodulation
- ➢ Automatic gain control
- ➢ Power measurement
- ➢ Voltage controlled amplifiers
- ➢ Frequency doublers

19. Discuss in detail the various applications of multiplier ICs. [May/June 2014][May/June 2012][April/May 2011].

4.6.5.1 Voltage Squarer

→ The simplest application of multiplier is voltage squarer.

→ When both inputs of multiplier tied together and applied with same input then, the resulting application is voltage squarer.

Inputs $V_x = V_y = V_i$

Output $V_o = k V_x V_y$

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$$= k. V_i^2$$

$$= \frac{1}{V_{ref}} . V_i^2 [\ K = \frac{1}{V_{ref}}, \text{ the scaling factor}]$$

$$V_0 = \frac{V_i^2}{V_{ref}}$$
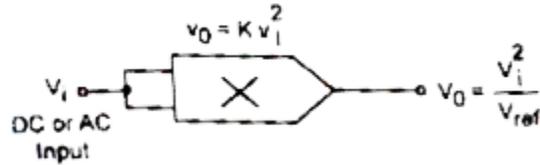
Figure 41: Voltage squarer

The above figure shows the voltage squarer using multiplier.

4.6.5.2 Frequency Doubler

→ The circuit diagram in fig (a) and the waveform diagram in fig (b) and expressions for a frequency doubler are given.

→ In this input signal $Vi = 5\sin 2\pi(10,000)t$; $A_v = 5$ V is the peak amplitude and 10k is the frequency in Hertz.

→ According to output voltage expression and substituting A_v and f, V_0 is given as

$$V_0 = \frac{A_V^2}{20}(1 - cos4\pi ft)$$

$$= \frac{(5)^2}{20}(1 - cos4\pi(10K)t)$$

$V_0 = 1.25 - 1.25 \cos 2\pi (20000) t$

(a) Circuit diagram

(b) Input and output waveforms
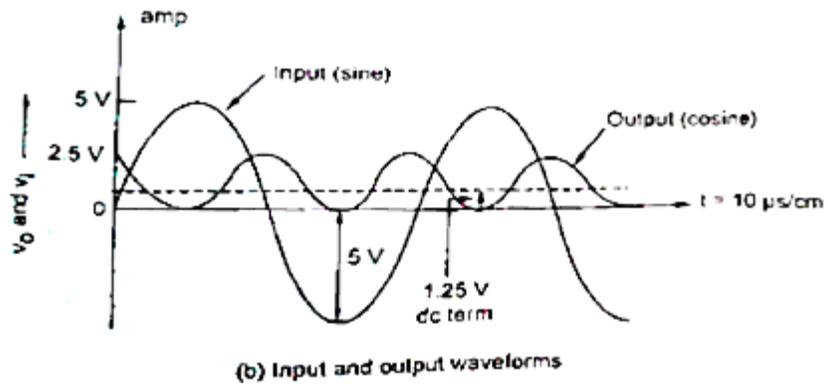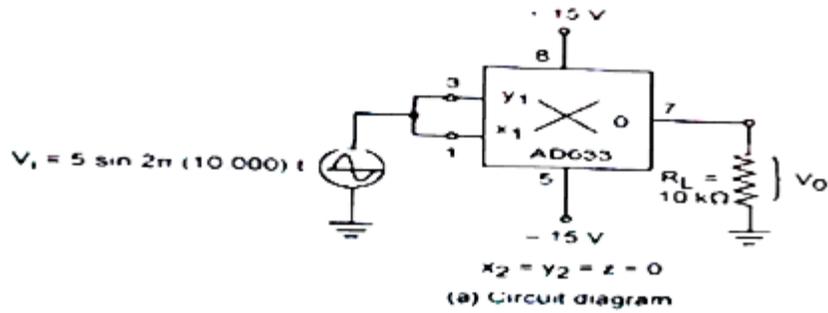
Figure 42: Frequency doubler

$$V_0 = \frac{A_V sin2\pi ft X A_V \ sin2\pi ft}{10}$$

$$= \frac{A_V^2}{10} sin^2(2\pi ft)$$

$$V_0 = \frac{A_V^2}{20}(1 - cos4\pi ft)$$

→ This input voltage V_0 is passed to a HPF to take ac term alone.

→ The first term 1.25 V represents the peak level of dc component and second term is the ac component.

→ The shape of the signal changes in the output from sine to cosine and note the amplitude of output decreases and frequency is doubled from 10 KHz to 20 KHz.

4.6.5.3 Voltage Divider

→ Voltage divider can be implemented by connecting a multiplier in the feedback loop of an op-amp as shown here in figure below.

V_{num} is the numerator voltage and V_{den} is the denominator voltage.

→ Note that node 'a' is at virtual ground and other end of R_c is physically grounded.
From the diagram,

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$i_1 + i_2 = 0$ and substituting $i_1 = \frac{V_{num}}{R}$; $i_2 = \frac{V_{om}}{R}$

$\frac{V_{num}}{R} + \frac{V_{om}}{R} = 0$

$\& V_{om} = k\, V_{OA} V_{den} = -V_{num}$

[Where V_{om} is output of multiplier with two inputs V_{OA} and V_{den}]

$$V_{OA} = \frac{-V_{num}}{KV_{den}}$$

K is the scale factor. Thus output V_{OA} from op-amp is the divided voltage.

Figure 43: Voltage divider

4.6.5.4 Square rooter

$\rightarrow$ The figure of divider circuit can be used as square rooter by connecting both inputs of the multiplier to the output of op-amp.

$V_{num} = k\, V_{OA} V_{den}$

$\& V_{OA} \& V_{den}$ are tied together we get,

$V_{OA} = V_{den} = V_0$ [V_0 is a common name assumed]

$$\because V_{num} = KV_0^2;$$

Take $k = \frac{1}{10}$ as scaling factor.

$V_0^2 = 10\, V_{num}$

$$V_0 = \sqrt{10|V_{num}|}$$

$\rightarrow$ Thus the output voltage is proportional to square root of V_{num} applied to inverting terminal of op-amp.

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4.6.5.5 Phase angle detector

→ The figure (a) shows the circuit and the figure (b) shows the input and output waveforms of phase angle detector using a multiplier.

(a) Circuit diagram
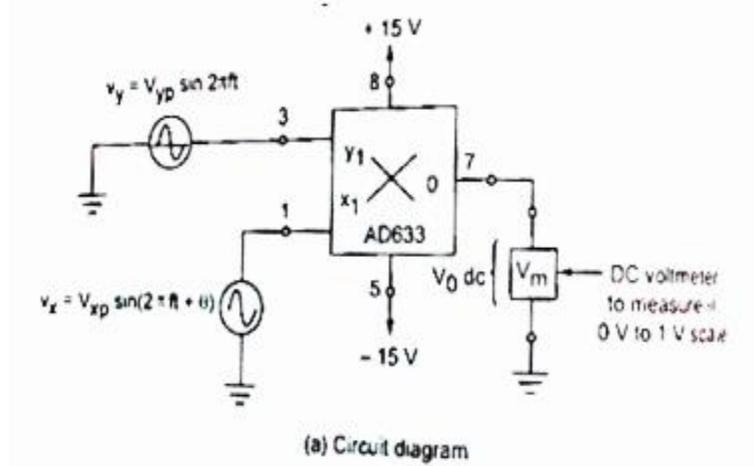
Figure 44: Phase angle detector

→ Two sine waves with same frequency are applied to multiplier.

→ They have different phase angles. The connection shown above in multiplier IC can be used to detect the phase angle difference between two input signals.

Using $\sin A \sin B = \frac{1}{2}(\cos(A\text{-}B)\text{- }\cos(A\text{- }B))$

$[\text{Sin }(2\pi ft + \theta)] \, [\text{Sin }(2\pi ft)] = \frac{1}{2}[Cos\theta - \cos(4\pi ft + \theta)]$

$$= \frac{1}{2}[\text{dc} - \text{ac frequency term}]$$

→ The output of multiplier is passed to a LPF which provides $\frac{1}{2}$dc as output. That is, $\frac{1}{2}\cos\theta$.

$$\therefore V_{O(dc)} = \frac{V_{xp}V_{yp}}{10}\left(\frac{1}{2}\cos\theta\right)$$

$$\therefore V_{O(dc)} = \frac{V_{xp}V_{yp}}{20}(\cos\theta)$$

→ The product V_{xp} V_{yp} is made to 20. So that output voltage is proportional to θ and the phase angle difference between two sinusoidal input voltages applied.

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$v_y = 4.47 \sin 2\pi(1000)t$

$v_x = 4.47 \sin(2\pi(1000)t + \theta)$

$\theta = 90°$

Input voltage for $\theta = 90°$

$v_0 = -\sin 2\pi(2000)t$

Output voltage for $\theta = 90°$; DC term is 0 V
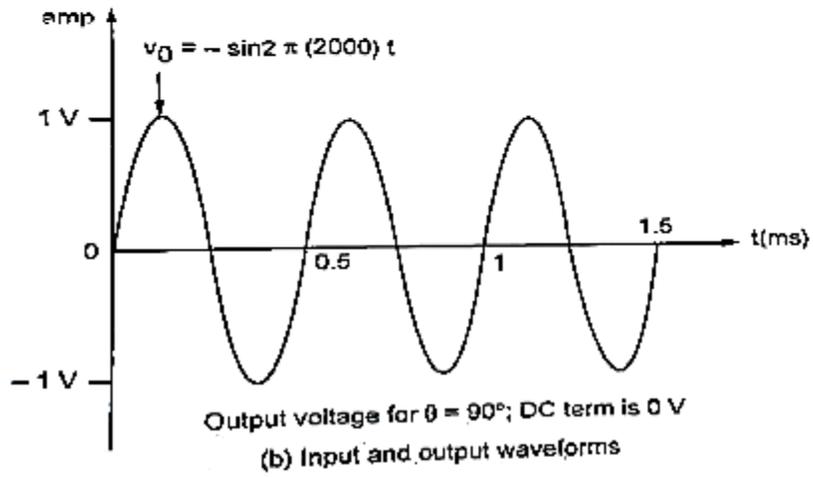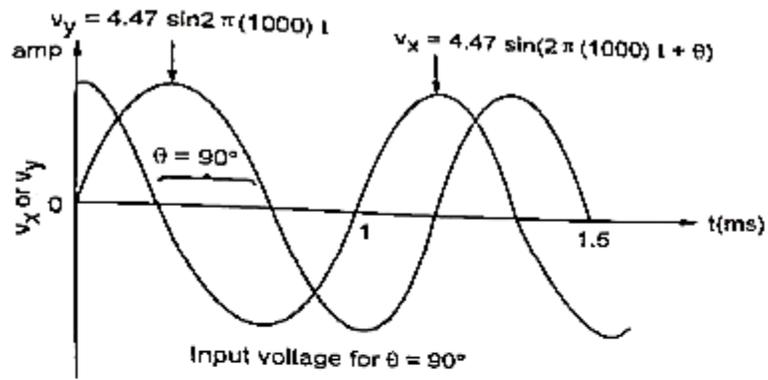
(b) Input and output waveforms

1. Name a few applications of an analog multiplier. [Nov/Dec 2009] [Apr/May 2017, 2018]

Applications of analog multiplier are:

- ❖ Frequency doubling.
- ❖ Frequency shifting.
- ❖ Phase angle detection.
- ❖ Squaring.
- ❖ Multiplication.
- ❖ Division.
- ❖ Waveform generation.

2. Define pull time of PLL.

Pull time of a PLL is defined as the total time taken by the PLL to establish lock.

3. What are the functional blocks of PLL? [April/May 2010]

The functional blocks of PLL are

- ❖ Comparator
- ❖ Low pass filter.
- ❖ Error amplifier.
- ❖ Voltage controlled oscillator.

4. Draw the functional block diagram of a PLL.
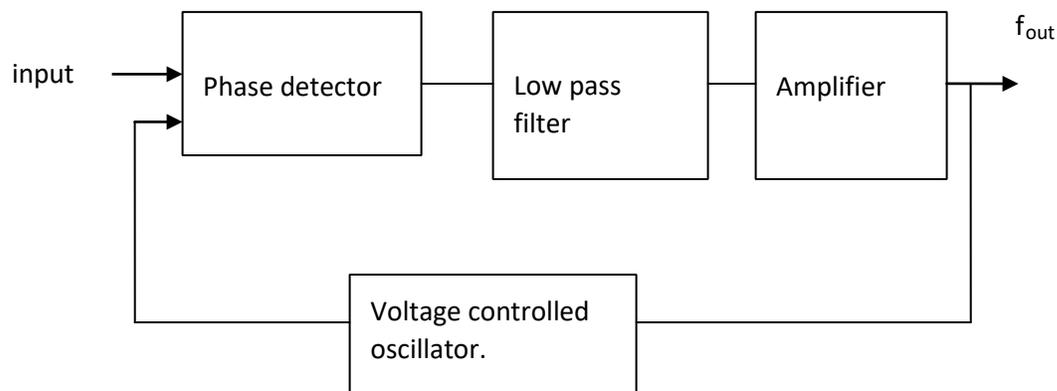
5. Draw circuit diagram of an AM detector using PLL. [May/June 2009]
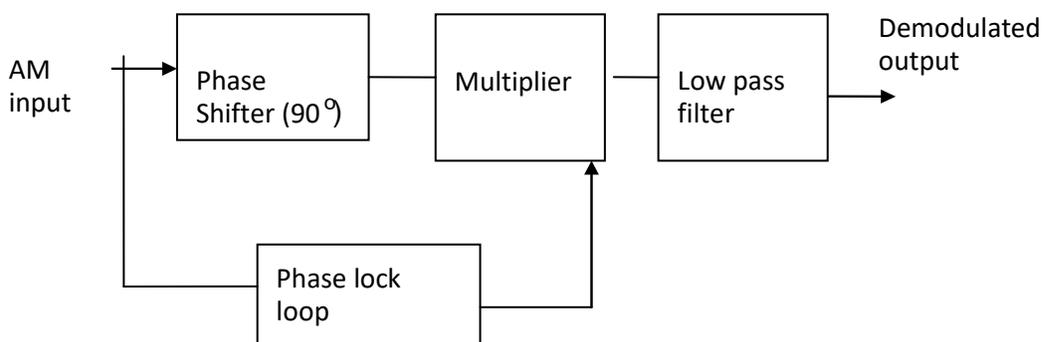
6. Mention a few applications of PLL. [Nov/Dec 2009] Nov/Dec 2019

The applications of PLL are:

- ❖ Frequency multiplication.
- ❖ Frequency division.
- ❖ AM detection.
- ❖ FM detection.
- ❖ FSK demodulator.
- ❖ Frequency translation.

7. Give the schematic symbol of multiplier.
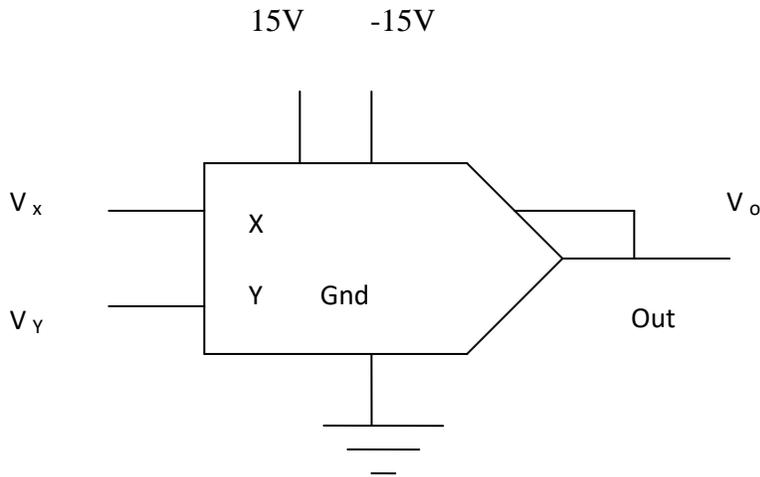
8. Define multiplier.

→ The multipliers are defined as circuits used for multiplying two applied signals.

→ Apart from this, multipliers can be used for phase angle detection, frequency doubling and shifting and for demonstrating the principle of amplitude modulation and demodulation.

9. Give the classification of multiplier.

The classifications of multipliers are:

- ❖ One-quadrant multiplier.
- ❖ Two- quadrant multiplier.
- ❖ Three - quadrant multiplier.
- ❖ Four- quadrant multiplier.

10. List the characteristics of multipliers.

The characteristics of multipliers are:

- ❖ Bandwidth.
- ❖ Feed through.
- ❖ Zero train.
- ❖ Quadrant.
- ❖ Scale factor.
- ❖ Scale-factor train.
- ❖ Accuracy.
- ❖ Linearity.

11. What is a trans-conductance multiplier?

  ❖ Log-amps require the input and reference voltages to be of the same polarity.
  ❖ This restricts log-antilog multipliers to one quadrant operation.
  ❖ A technique that provides four quadrant multiplication is called trans-conductance multiplier.

12. What is four quadrant multiplier?

  ❖ If both inputs are positive, the IC is said to be a one-quadrant multiplier.
  ❖ A two- quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative.
  ❖ If both inputs are either positive or negative, the IC is called a four quadrant multiplier.

13. List the various multiplier techniques.

The various multiplier techniques are:

  ❖ Logarithmic multipliers
  ❖ Quarter square multipliers
  ❖ Pulse width/height modulation multipliers
  ❖ Variable trans-conductance multipliers.

14. What is the range of modulating input voltage applied to a voltage controlled oscillator?

The modulating input voltage ranges from 0.75Vcc to Vcc.

15. Define VCO.

  ❖ The VCO is a free running multivibrator and operates at a set frequency called free running frequency.
  ❖ This frequency is determined by an external timing capacitor and an external resistor.

16. List the features of VCO.

The features of VCO are:

  ❖ Wide supply voltage range from 10V to 24V.
  ❖ Very linear modulation characteristics.
  ❖ High temperature stability.
  ❖ Excellent power supply rejection.
  ❖ 10 to 1 frequency range with fixed C.
  ❖ The frequency can be controlled by means of a control voltage resistor or capacitor.

17. Give the applications of VCO.

The applications of VCO are:

  ❖ FM modulation.

  ❖ Signal generation(triangular or square wave)

  ❖ Function generation.

  ❖ In frequency multipliers.

  ❖ Converting low frequency signals such as EEG and ECG into audio frequency range signals.

18. What are the different stages of operation in a PLL?

The different stages of operation in a PLL are,

❖ Free running range.
❖ Capture range.
❖ Locked or tracking range.

19. Define lock-in range [April/May 2008, 2018] [Nov/Dec 2015]

The range of frequency over which the PLL can maintain lock with the incoming signal is called the lock-in range.

20. What is meant by capture range of PLL? [April/May 2008, 2018] [Nov/Dec 2015]

The range of frequency over which the PLL can acquire lock with an input signal is called capture range.

21. Give the types of analog phase detectors and digital phase detectors.

The types of analog phase detectors are as follows:

❖ Switch type phase detector.
❖ Balanced modulator type phase detector.

The types of digital phase detectors are as follows:

❖ X-OR phase detector.
❖ Flip-flop phase detectors.

22. List the advantages of flip-flop type phase detector over EX-OR phase detector.

The flip flop phase detector has the following advantages over the EX-OR circuit:

❖ The dc output voltage is linear over 2π radians or 360°, as opposed to π or 180° in the case of EX-OR detector.
❖ The flip-flop detector exhibits between capture, tracking, and locking characteristics than the EX-OR detector.
❖ The RS flip-flop works best with low duty cycle(50%) input waveform. However both the types of detectors are sensitive to harmonics of the input signal and change in duty cycle of f_i and f_o.

23. What should be the phase difference between the input signal and voltage controlled oscillator output to active lock?

Input signal and voltage controlled oscillator should be 90° out of phase with each other.

24. Define amplitude modulation. [April/May 2005]

The amplitude of a high frequency carrier wave is varied in accordance with the message signal (input signal) and this process is called modulation.

25. Define demodulation.

Demodulation or detection is the process of recovering a modulating signal E_m from the modulated output voltage V_o.

26. What is the need for amplitude modulation?

The need for amplitude modulation is:

❖ Low frequency audio or data signals cannot be transmitted from antenna of reasonable size.

- ❖ Changing or modulating some characteristics of higher frequency carrier wave can transmit audio signals.
- ❖ Changing the frequency of the carrier is changed in proportion to the audio signal, the process is called amplitude modulation (AM).
- ❖ Changing the frequency or the phase angle of the carrier wave results in frequency modulation (FM) and phase angle modulation (PM) respectively.
- ❖ The original audio signal must be recovered by a process called demodulation or detection.

27. Define FSK techniques. [Nov/Dec 2009]

- ❖ During digital data transmission, binary code is transmitted by shifting a carrier frequency between two frequencies.
- ❖ This type of transmission is called frequency shift keying technique.

28. A PLL has a free running frequency of 500 kHz and bandwidth of the low pass filter is 10 kHz. Will the loop acquire lock for an input signal of 600 kHz? Justify your answer. Assume that the phase detector produces 50 m and difference frequency components.

The phase detector output

$$f_i + fc = 600 \text{ kHz} + 500 \text{ kHz}$$
$$= 1100 \text{ kHz}$$

$$f_i - fc = 600 \text{ kHz} + 500 \text{ kHz}$$
$$= 100 \text{ kHz}$$

As both the components are outside the pass band of low pass filter, the loop will not acquire lock.

29. What is modulation?

Some characteristics of the carrier wave change in accordance with the instantaneous value of a incoming signal or modulating signal.

30. Give the advantages of variable Transconductance technique.

The advantages of variable Transconductance technique are,

- ❖ Good accuracy.
- ❖ Economical.
- ❖ Simple to integrate into monolithic chip.
- ❖ Higher bandwidth.

31. What is companding?

- → The combination of words compression and expanding in a communication system is called companding.
- → The compression is done in the transmitter and expanding is done in the receiver.

32. What is the purpose of companding?

The purpose of companding is to preserve the signal to noise ratio of the original signal and to avoid nonlinear distortion of the signal when the input amplitude is large.

33. Define scale factor of multiplier.

Scale factor is proportionally constant (k) relating the output voltage and the product of two input voltage.

$k = (V_o / V_1 V_2)$.

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34. Name two applications of PLL. [May 2004]

Some of the applications of PLL are,

❖ Frequency multiplier.
❖ Frequency shift keying (FSK) demodulator.
❖ Frequency translation.
❖ Frequency synthesizer.
❖ AM detection.
❖ FM detection.

35. What is an OTA?

An OTA (Operational Transconductance amplifier) is a voltage-input current output amplifier.

36. What is missing pulse detector?

The IC 555 timer can able to detect the missing pulses in the trigger input pulses.

37. Give the output for missing pulse detector. [Apr/May 2019]
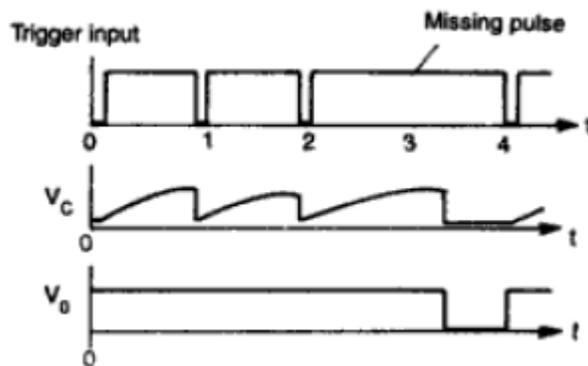
38. What is the need for frequency synthesizer? [May/June 2014]

❖ The frequency synthesizer is used to produce a large number of precise frequencies which are derived from a single reference source of frequency.

❖ The reference source usually is a crystal oscillator.

39. What are advantages of emitter coupled transistor pair? [April/ May 2011]

The advantages of emitter coupled transistor pair are,

❖ High current gain
❖ More stability
❖ Compact and easily implemented in IC

40. What is 555 timer?

The device 555 timer is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillations. Like general purpose op- amps, the 555 timer is reliable, easy to use and economical.

41. List the modes of operation of 555 timer.

❖ As table mode of operation
❖ Mono stable mode of operation

42. List the important basic building blocks of 555 timer.

❖ A relaxation oscillator
❖ R-S flip- flop

❖ Two comparators

❖ Discharge transistors

43. Mention some areas where PLL is widely used.

❖ Radar synchronisation

❖ Satellite communication systems

❖ Air borne navigational system

❖ Com

❖ puters

44. Give the classification of phase detector.

❖ Analog phase detector

❖ Digital phase detector

45. Define pull- in time.

The total time taken by the PLL to establish lock is called pull- in time. It depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

46. Determine the frequency of oscillations, if the duty cycle D-20% and the ON period T_{ON} =2ms. [Apr/May 2019]

$\%D = W/TX100\%$

$W= T_{ON} = 2ms$

$D=20\%$

Frequency of oscillation f=1/T

$$= 1/0.693(R_A+2R_B)C$$

$$= 1.44/(R_A+2R_B).C$$

47. What is Astable Multivibrator? Nov/Dec 2019

The Astable Multivibrator has no stable state, and the trigger is not required to change the state, hence free running.

48. In a Monostable Multivibrator using 555 timer, the components values are RA= 5.6 Ω and C= 0.068 µF. Find the pulse width period T. Nov/Dec 2019

RA= 5.6 Ω; C= 0.068 µF

T= 1.1 RC (Seconds)

T= 1.1 x 5.6Ω x 0.068 µF

T= 0.42

UNIT – V

APPLICATION ICs

AD623 Instrumentation Amplifier and its application as load cell weight measurement – IC voltage regulators – LM78XX - LM79XX - Fixed voltage regulators its application as Linear power supply - LM317, 723 Variability voltage regulators, switching regulator - SMPS – ICL 8038 function generator IC.

5.1 AD623 INSTRUMENTATION AMPLIFIER AND ITS APPLICATION AS LOAD CELL WEIGHT MEASUREMENT

1. Explain in detail about AD623 instrumentation amplifier.

The AD623 is an instrumentation amplifier based on the three op-amp in-amp circuit, modified to assure operation on either single or dual power supplies, even at common-mode voltages at or even below the negative supply rail (or below "ground" in single supply operation).

5.1.1 Features:

➢ Rail-to-rail output voltage swing

➢ Low supply current

➢ Micro SOIC packaging

➢ Low input and output voltage offset

➢ Microvolt/dc offset level drift

➢ High common-mode rejection

➢ Only one external resistor to set the gain.
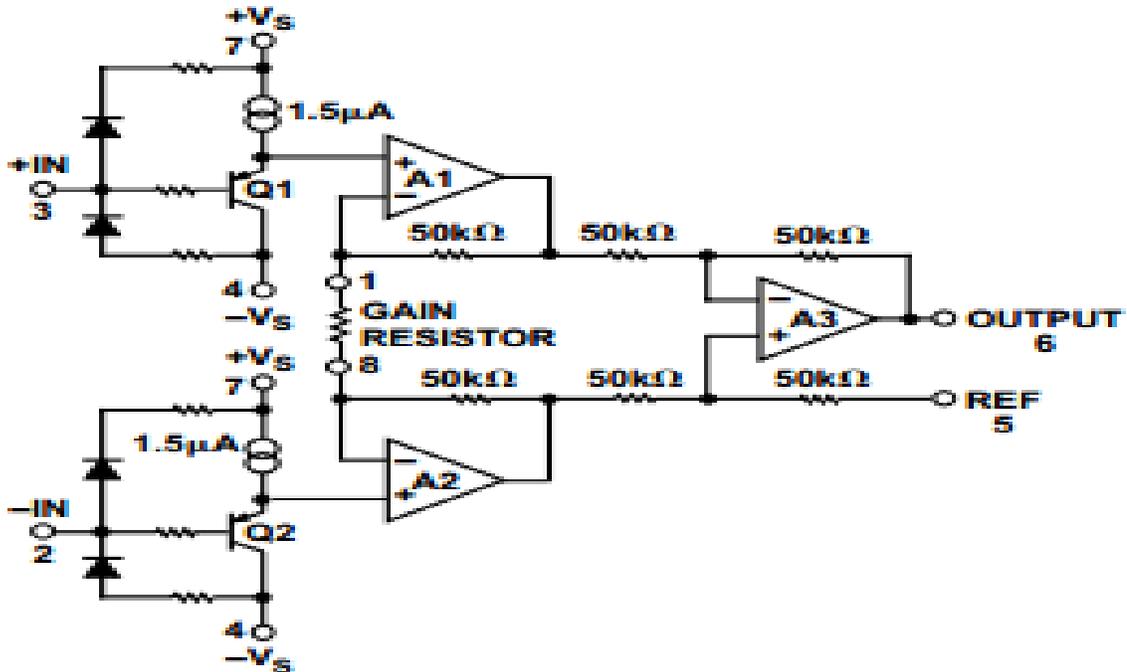
Figure 1: AD623 Simplified Schematic

→ The input signal is applied to PNP transistors acting as voltage buffers and dc level-shifters A resistor trimmed to within 0.1% of 50 kΩ in each amplifiers' (A1 and A2) feedback path assures accurate gain programmability.

→ The differential output is:

$$V_O = \left(1 + \frac{100\ k\Omega}{R_G}\right) + V_C$$

where RG is in kΩ.

→ The differential voltage is then converted to a single ended voltage using the output difference amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

→ Since all the amplifiers can swing to either supply rail, as well as have their common mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced.

→ Note that the base currents of Q1 and Q2 flow directly "out" of the input terminals, unlike dual supply input current compensated in-amps such as the AD620.

2

→ Since the inputs (i.e., the bases of Q1 and Q2) can operate at "ground" i.e., 0 V (or, more correctly, at 200 mV below ground), it was not possible to provide input current compensation for the AD623.

→ However, the input bias current of the AD623 is still very small: only 25 nA max.

→ The output voltage at Pin 6 is measured with respect to the "reference" potential at Pin 5. The impedance of the reference pin is 100 kΩ.

→ Internal ESD clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand over voltages of 0.3 V above or below the supplies.

→ This is true for all gains, and with power on or off.

→ If the overvoltage is expected to exceed this value, the current through these diodes should be limited to 10 mA, using external current limiting resistors.

→ The value of these resistors is defined by the in-amp's noise level, the supply voltage, and the required overvoltage protection needed.

→ The bandwidth of the AD623 is reduced as the gain is increased, since A1 and A2 are voltage feedback op-amp.

→ However, even at higher gains, the AD623 still has enough bandwidth for many applications.

→ Figure shows the gain vs. frequency of the AD623. The AD623 is laser- trimmed to achieve accurate gains using 0.1% to 1% tolerance resistors.
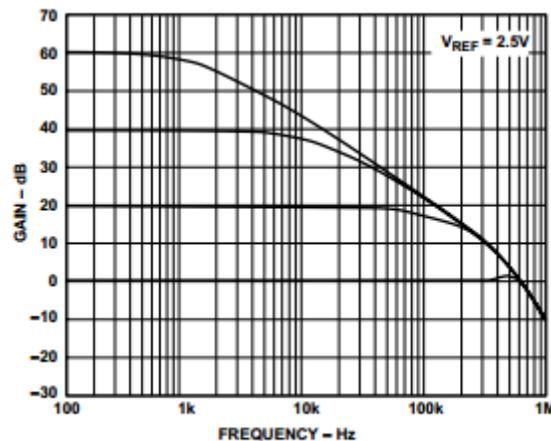

Figure 2: AD623 Closed-Loop Gain vs. Frequency

5.2 IC VOLTAGE REGULATORS

5.2.1 Introduction to special function ICs

Special function ICs are used for special purpose or for particular application. In contrast, general purpose ICs finds applications in many areas. Example of general purpose ICs include op-amp, logic gate ICs, multipliers etc. some of the special function ICs and its purpose is listed here.

➢ Function generator IC – 8038, XR 2206, 566 (VCO)

➢ Timer IC – 555, XR 2240

➢ Monolithic IC voltage regulator – IC 7840, MC 3420, SG 1524

➢ Three terminal voltage regulators (fixed or variable and positive or negative) – 78XX, 79XX, LM317, LM337, LM2577

➢ General purpose voltage regulator – LM 723, MC 1723

➢ Switched capacitor filter IC – MF 5, MF 10, FLT – U2

➢ Frequency to voltage (or) voltage to frequency converters – VFC 32, IC 9400

➢ Audio power amplifier – LM 380, ICH 8510, LM 337, µA 706, TDA 2002, LM 379

➢ Video power amplifier – IC 733, 3040, MC 1550

➢ Isolation amplifier – ISO 100

➢ Opto couplers – TLP series, MOC series, MCT2E

➢ Fiber optic IC – IOM – chip, LASER DRIVER 3738 IC

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2.   What do you mean by the fixed voltage and variable voltage regulator? List its various applications. (13) [Nov/Dec 2016]

(or)

Explain the working principle of basic linear voltage regulator using op- amp. (May 2018) (7)

→ All electronic circuits need a dc power supply for their operation.

→ To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.

→ Therefore the filters are used to obtain a ―steady‖ dc voltage from the pulsating one.

→ The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.

→ We know the combination of rectifier & filter can produce a dc voltage.

→ But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an ac input or changes in the load current(IL).

→ The output of unregulated power supply is connected at the input of voltage regulator circuit.

→ The voltage regulator is a specially designed circuit to keep the output voltage constant.

→ It does not remain exactly constant. It changes slightly due to changes in certain parameters.

5.2.2 Factors affecting the output voltage:

→ I_L (Load Current)

→ V_{IN} (Input Voltage)

→ T (Temperature)

5.2.3 IC Voltage Regulators:

→ They are basically series regulators with all the basic blocks present inside the IC.

→ Therefore it is easier to use IC voltage regulator instead of discrete voltage regulators.

5.2.4 Important features of IC Regulators:

➢ Programmable output

➢ Facility to boost the voltage/current

➢ Internally provided short circuit current limiting

➢ Thermal shutdown

➢ Floating operation to facilitate higher voltage output

5.2.5 Classifications of IC voltage regulators:

→ IC voltage regulators are classified into following types,

➢ Fixed positive and/or negative output voltage regulators

➢ Adjustable positive and/or negative output voltage regulators

➢ Switching regulators

➢ Special regulators

→ Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.

→ A series pass transistor is used and it operates always in its active region.

5.2.6 Switching Regulator:

→ Series Pass Transistor acts as a switch.

→ The amount of power dissipation in it decreases considerably.

→ Power saving result is higher efficiency compared to that of linear.

5.2.7 Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

→ Adjustable output voltage from 1.2v to 57 v

→ Output current 0.10 to 1.5 A

5

→ Better load & line regulation

→ Improved overload protection

→ Improved reliability under the 100% thermal overloading

5.3 Three terminal voltage regulators

5.3 Fixed voltage regulators with three terminals

5.3 78XX: (Positive voltage regulator)

3. Explain the fixed voltage regulator and its applications. Apr/ May 2019

(or)

Discuss with neat diagram, the working of IC 7805 regulator as

(i)   Current source
(ii)   Boosting regulator output current
(iii)   IC 7805 regulator as current source. Nov/Dec 2019

→ It is a three terminal positive voltage regulator with seven voltage options.

→ These ICs are designed as fixed voltage regulators and with adequate heat sinking, can deliver current in excess of 1A.

→ External components can be used to obtain variable output.

→ These ICs also have internal thermal overload protection and internal short-circuit current limiting.

→ The prefix number '78' indicates the regulator is a positive voltage regulator and letters 'XX' indicate the magnitude of output voltage.

→ This is shown in table below.

Series of Possible output voltages [Apr/May2019]

Device type	Output voltage(v)	Maximum input voltage(v)
7805	5.0	
7806	6.0	
7808	8.0	
7812	12.0	35
7815	15.0	
7818	18.0	
7824	24.0	40

The available packages are shown in fig (a) and (b).

5.3.1 Package types
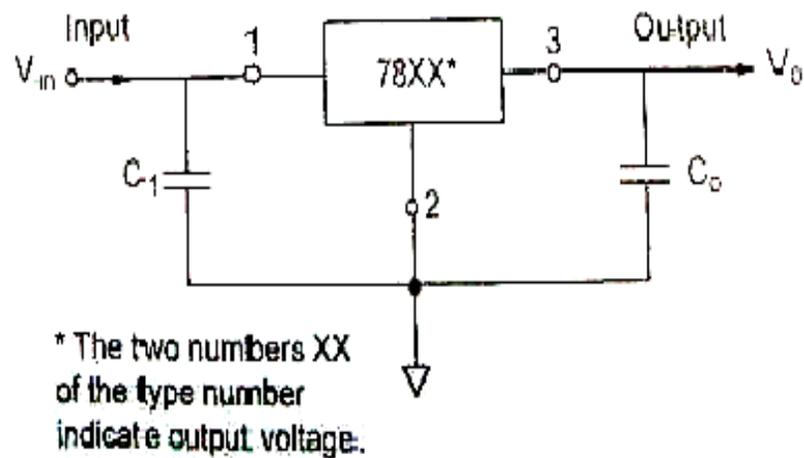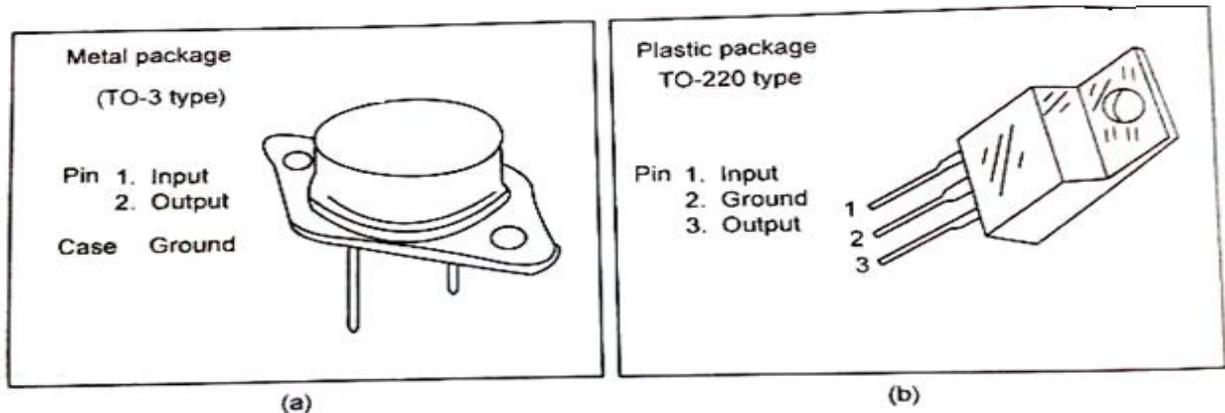
Figure 3: Package types

→ The application diagram of IC7800 series regulators are shown in figure below.

→ Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection.

5.3.2 Line or Input regulation

→ It is defined as the change in output voltage for a change in input voltage and is usually expressed in mill volts or as a percentage of output voltage V_0.

5.3.3 Load regulation

→ It is defined as the change in output voltage for a change in load current and is also expressed in milli volts or as a percentage of V0. 7805 indicates V0 = +5V.

→ 7800 ICs can also be used as current sources. **Example:** 0.5A current source is shown in figure below.

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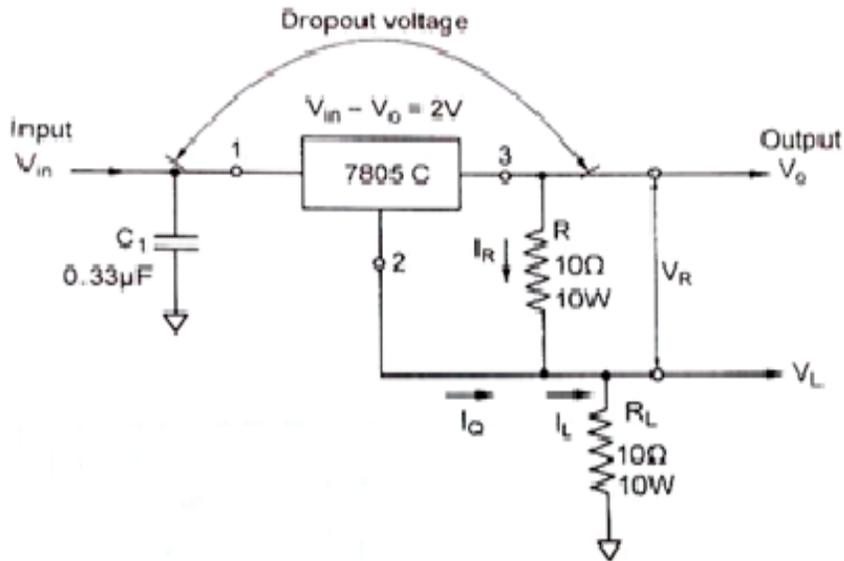
Figure 4: Load regulator

5.4 79XX (Negative voltage regulator)

→ It is a three terminal negative voltage regulator with nine voltage options.

→ The two voltage extra options than in 78XX are -2V and -5.2V available in 79XX.

→ The prefix '79' indicates negative and 'XX' indicates the magnitude of output voltage.

  ☐**Example:** 7912 produces -12V as regulated output voltage.

→ The voltage options are shown in table below.

5.4.1 Series of possible output voltages [Apr/May2019]

Device type	Output voltage(v)	Maximum input voltage(v)
7902	-2.0	
7905	-5.0	
7905.2	-5.2	
7906	-6.0	
7908	-8.0	-35
7912	-12.0	
7915	-15.0	
7918	-18.0	
7924	-24.0	-40

→ There were two popular packages available for 79XX as shown here in fig (a) and fig (b)

8
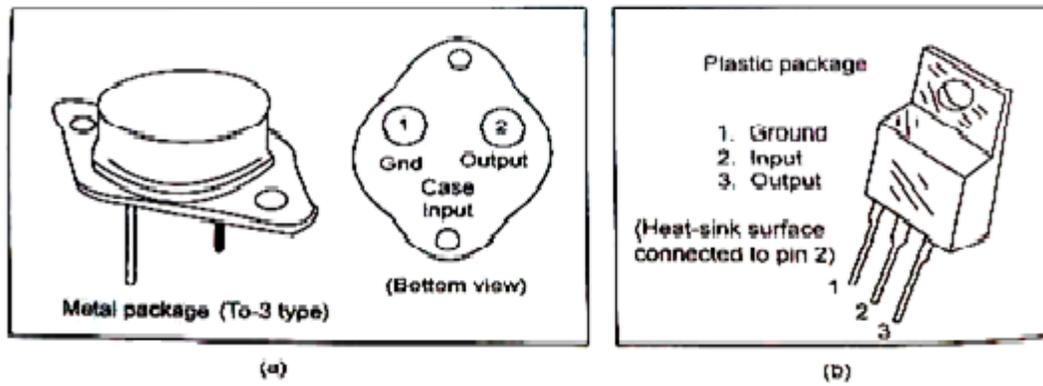
5.4.2 Package types

Figure 5: Package types

→ 78XX and 79XX are mostly used as fixed output voltage regulators in most of the linear power supplies.

5.4.3 Three terminal adjustable voltage regulators

→ Adjustable voltage regulators are single devices that satisfy many voltage requirements from 1.2V to 57V.

→ They have the following advantages over fixed voltage regulators. T

→ hey are improved system performance by having line and load regulation of a factor of 10 or better.

→ Improved overload protection allows greater output current over operating temperature range.

→ Improved system reliability with each device being subjected to 100% thermal limit burn-in.

5.5 Adjustable Positive Voltage Regulator (LM317):

$\rightarrow$ It is most popular and widely used general purpose adjustable voltage regulator.

$$V_o = 1.25V\left(1 + \frac{R_2}{R_1}\right)$$
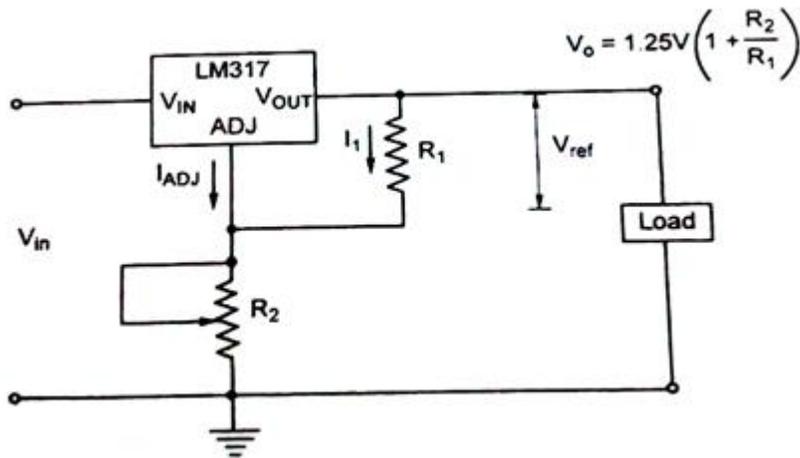
Figure 6: LM 317- Voltage regulator

$\rightarrow$ LM317 series are adjustable 3 terminal positive voltage regulators. The three terminals are V_{in}, V_{out} & adjustment (ADJ).

$\rightarrow$ LM317 requires only 2 external resistors to set the output voltage.

$\rightarrow$ LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as V_{ref}.

$\rightarrow$ V_{ref} (Reference Voltage) is a constant; hence current I1 flows through R1 will also be constant.

$\rightarrow$ Because resistor R_1 sets current I_1. It is called ―current set or ―program resistor.

$\rightarrow$ Resistor R_2 is called as ―Output set resistors, hence current through this resistor is the sum of I_1 & I_{adj}

$\rightarrow$ LM317 is designed in such as that I_{adj} is very small & constant with changes in line voltage & load current.

$\rightarrow$ The output voltage V_0 is, $V_0 = R_1 I_1 + \left(I_1 + I_{adj}\right)R_2$ $\qquad - - - - - - - (1)$

$$\text{Where } I_1 = V_{ref}/R_1$$

$$V_0 = \left(V_{ref}/R_1\right)R_1 + V_{ref}/R_1 + I_{adj}R_2$$

$$= V_{ref} + \left(V_{ref}/R_1\right)R_1 + I_{adj}R_2 + I_{adj}R_2$$

$$V_0 = V_{ref}[1 + R_2/R_1] + I_{adj}R_2 - - - - - - - (2)$$

R_1 = Current (I_1) set resistor

R₂ = output (Vo) set resistor

→ V_{ref} = 1.25v which is a constant voltage between output and ADJ terminals.
→ Current I_{adj} is very small. Therefore the second term in (2) can be neglected.
→ Thus the final expression for the output voltage is given by

$$V_0 = 1.25V[1 + R_2/R_1] \qquad\qquad ------- (3)$$

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2. The value of R1 is normally kept constant at 240 ohms for all practical applications.

5.5.1 Practical Regulator using LM317:
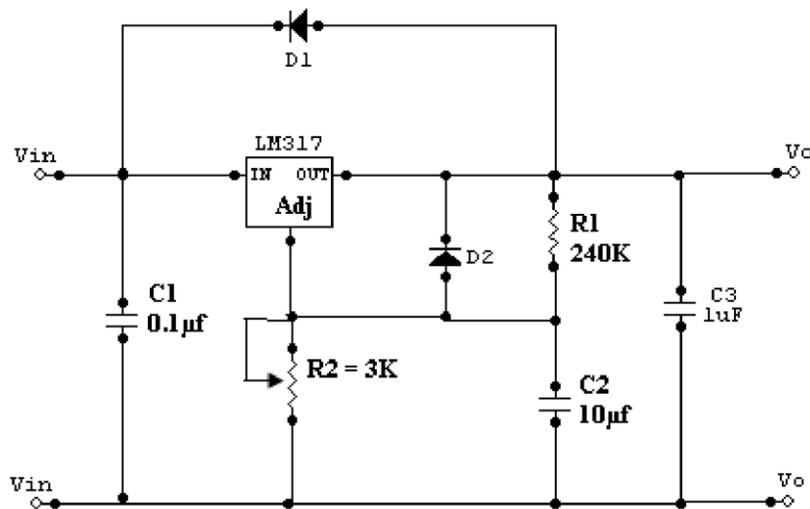
Figure 7: Practical voltage regulator

→ If LM317 is far away from the input power supply, then 0.1μf disc type or 1μf tantalum capacitor should be used at the input of LM317.

→ The output capacitor Co is optional. Co should be in the range of 1 to 1000μf.

→ The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.

→ When the filter capacitor is used, it is necessary to use the protective diodes.

$\rightarrow$ These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.

$\rightarrow$ These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25μf and above.

5.6 <u>IC 723 – GENERAL PURPOSE REGULATOR</u>

4. **Discuss in detail about general purpose regulator. (8) [Nov/Dec 2015] [May/June 2013] [May/June 2012]**

    (or)

    Elaborate with neat diagram, the working of IC 723 as low voltage and high voltage regulators. Nov/Dec 2019

$\rightarrow$ IC 723 is a monolithic general purpose voltage regulator used to produce variable output voltage with positive and negative polarity.

  a. It overcomes the drawbacks present in three terminal voltage regulators.

5.6.1 <u>Disadvantages of fixed voltage regulator:</u>

  $\triangleright$ Do not have the shot circuit protection
  $\triangleright$ Output voltage is not adjustable

These limitations can be overcomes in IC723.

5.6.2 <u>Features of IC723:</u>

  $\triangleright$ Unregulated dc supply voltage at the input between 9.5V & 40V.
  $\triangleright$ Adjustable regulated output voltage between 2 to 3V.
  $\triangleright$ Maximum load current of 150 mA ($I_{Lmax} = 150mA$).
  $\triangleright$ With the additional transistor used, I_{Lmax} upto 10A is obtainable.
  $\triangleright$ Positive or Negative supply operation
  $\triangleright$ Internal Power dissipation of 800mW.
  $\triangleright$ Built in short circuit protection.
  $\triangleright$ Very low temperature drift.
  $\triangleright$ High ripple rejection.
  $\triangleright$ The simplified functional block diagram can be divided in to 4 blocks.
  $\triangleright$ Reference generating block
  $\triangleright$ Error Amplifier
  $\triangleright$ Series Pass transistor
  $\triangleright$ Circuitry to limit the current

5.6.3 Reference Generating block:

→ The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block.

→ The Zener diode is used to generate a fixed reference voltage internally.

→ Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier.

→ The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

5.6.4 Error Amplifier:

→ Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting).

→ The Non-inverting terminal is connected to the internally generated reference voltage.

→ The Inverting terminal is connected to the full regulated output voltage.
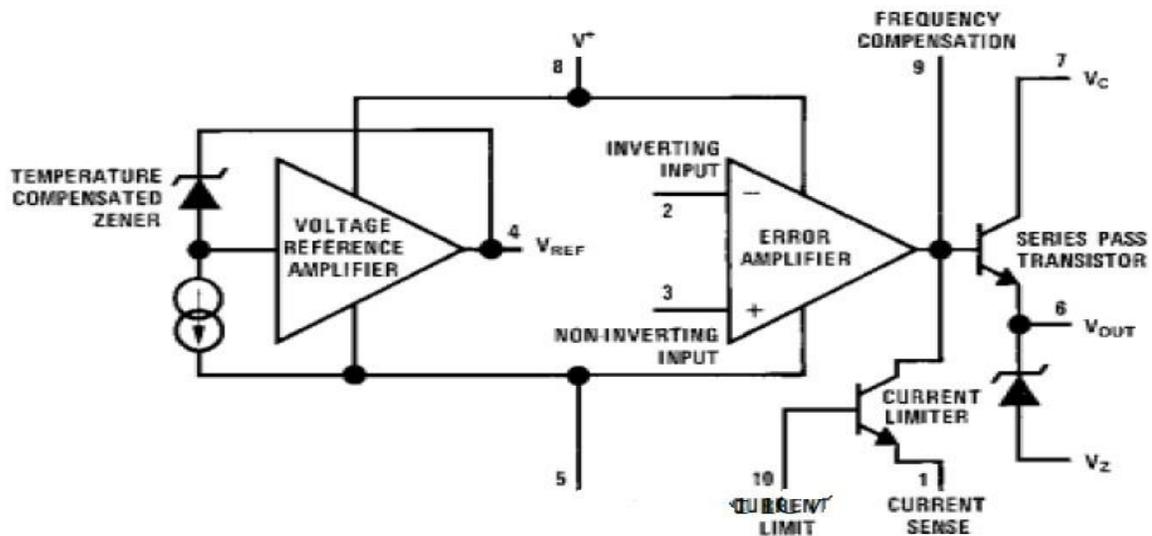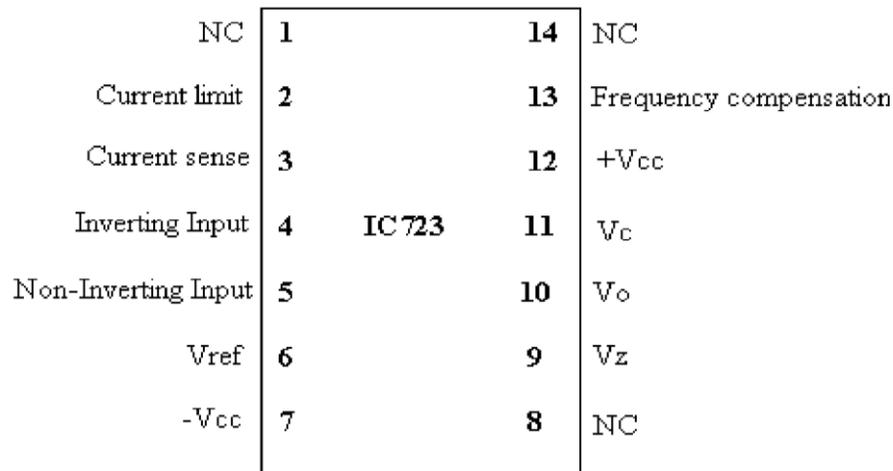
Figure 8: Functional block diagram of IC723

NC	1		14	NC
Current limit	2		13	Frequency compensation
Current sense	3		12	+Vcc
Inverting Input	4	IC 723	11	Vc
Non-Inverting Input	5		10	Vo
Vref	6		9	Vz
-Vcc	7		8	NC

Fig 9: Pin diagram of IC723

5.6.5 Series Pass Transistor:

→ Q1 is the internal series pass transistor which is driven by the error amplifier.

→ This transistor actually acts as a variable resistor & regulates the output voltage.

→ The collector of transistor Q1 is connected to the Un-regulated power supply.

→ The maximum collector voltage of Q1 is limited to 36Volts.

→ The maximum current which can be supplied by Q1 is 150mA.

5.6.6 Circuitry to limit the current:

→ The internal transistor Q2 is used for current sensing & limiting.

→ Q2 is normally OFF transistor.

→ It turns ON when the IL exceeds a predetermined limit.

→ Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.

V_{load} = 2 to 7V

I_{load} = 150mA

5.6.7 Applications of 723 voltage regulator

LM723 voltage regulator can be used as

→ Low voltage regulator

→ High voltage regulator

→ Current booster

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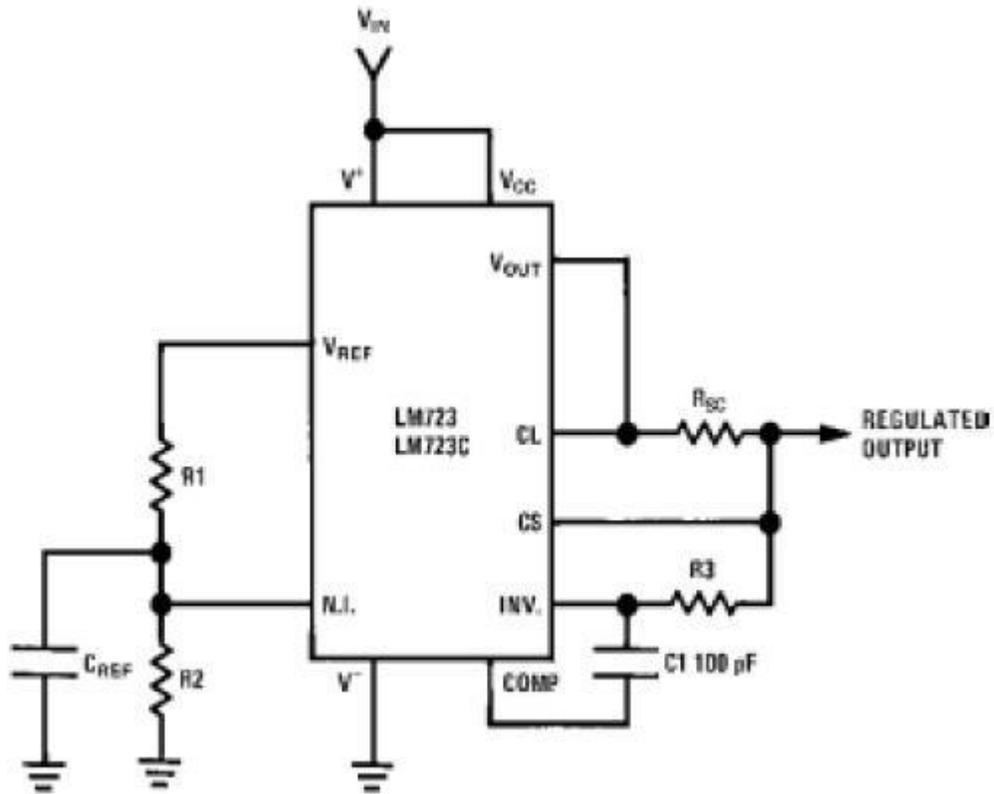
Fig10: Typical circuit connection diagram

$\rightarrow$ R_1 & R_2 from a potential divider between V_{ref} & Gnd.

a. The Voltage across R_2 is connected to the Non – inverting terminal of the regulator IC.

$$V_{non-inv} = \frac{R_2}{R_1 + R_2} V_{ref}$$

b. Gain of the internal error amplifier is large

   $V_{non-inv} = V_{in}$

c. Therefore the Vo is connected to the Inverting terminal through R3 & RSC must also be equal to Vnon-inv

$$V_0 = V_{non-inv} = \frac{R_2}{R_1 + R_2} V_{ref}$$

d. R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

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e. R_{sc} (current sensing resistor) is connected between Cs & CL. The voltage drop across Rsc is proportional to the I_L.

f. This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.

g. The current sourcing capacity is increased by including a transistor Q in the circuit.

h. The output voltage, $V_0 = \frac{R_2}{R_1+R_2} V_{ref}$

IC723 as a HIGH voltage LOW Current:

i. This circuit is capable of supplying a regulated output voltage between the ranges of 7 to 37 volts with a maximum load current of 150 mA.

j. The Non – inverting terminal is now connected to V_{ref} through resistance R_3.

k. The values of R_1 & R_2 are adjusted in order to get a voltage of V_{ref} at the inverting terminal at the desired output.

$$V_{in} = V_{ref} = \frac{R_2}{R_1 + R_2} V_0$$

$$V_0 = \frac{R_1 + R_2}{R_2} V_{ref}$$

$$V_0 = \left[1 + \frac{R_1}{r_2}\right] V_{ref}$$
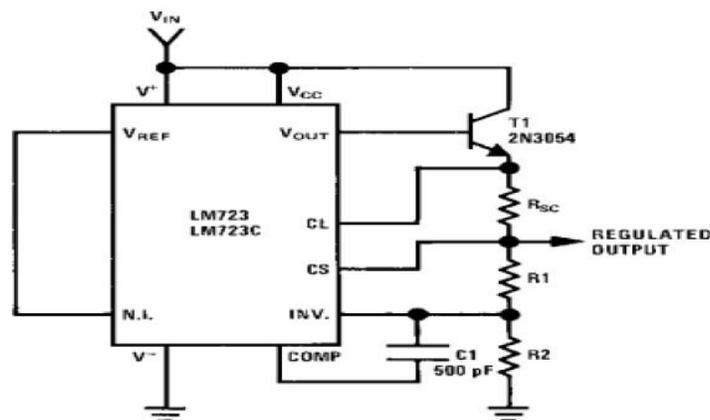
IC723 as a HIGH voltage HIGH Current:

Fig 11: Typical circuit connection diagram

16

l. An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.

m. For this circuit the output voltage varies between 7 & 37V.

n. Transistor Q increase the current sourcing capacity thus $I_L(MAX)$ is greater than 150mA.

o. The output voltage Vo is given by ,

$$V_0 = (R_2/R_1+R_2)\ V_{ref}$$

→ The value of R_{sc} is given by $R_{sc} = \dfrac{0.6}{I_{Limit}}$

5.7 SWITCHING REGULATOR:

6. **Discuss in detail about switching regulator. (8) [April/May 2018] [April/May2017][April/May 2015][April/May 2014] [APR/MAY2019]**

a. An example of general purpose regulator is Motorola's MC1723.

b. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

c. To minimize the power dissipation during switching, the external transistor used must be a switching power transistor.

d. To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

e. A regulator constructed to operate in this manner is called a series switching regulator.

f. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.

g. This output is filtered through a low pass LC filter to produce an average dc output voltage.

h. Thus the output voltage is proportional to the pulse width and frequency.

i. The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%.
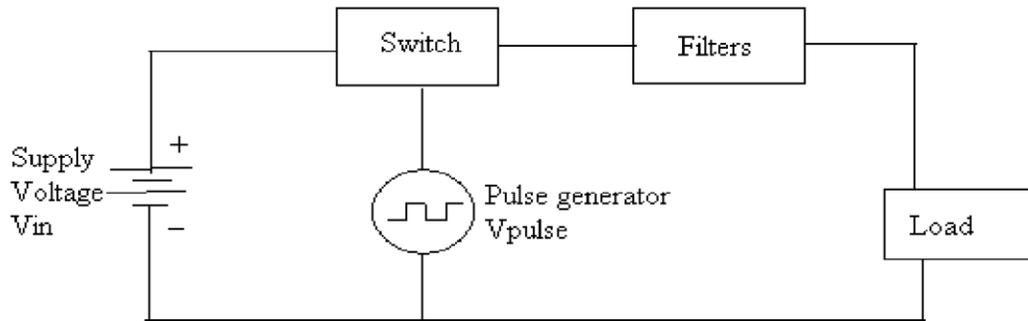
Fig 12: Basic Switching regulator

A basic switching regulator consists of 4 major components,

> ➤ Voltage source V_{in}

> ➤ Switch S1

> ➤ Pulse generator V_{pulse}

> ➤ Filter F1

1. Voltage Source Vin:

     It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

→ It must supply the required output power & the losses associated with the switching regulator.

→ It must be large enough to supply sufficient dynamic range for line & load regulations.

→ It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.

→ It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

→ It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode.

→ The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator V pulse:

→ It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively.

→ The most effective frequency range for the pulse generator for optimum efficiency 20 KHz.

→ This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

→ The duty cycle of the pulse wave form determines the relationship between the input & output voltages.

→ The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

$$Duty\ cycle = \frac{t_{on}}{t_{on} + t_{off}}$$

→ Switching regulator can operate in any of 3 modes.

$$= \frac{t_{on}}{T} = t_{off}$$

Where ton = On-time of the pulse waveform

Toff = off-time of the pulse wave form

T = time period = ton + toff

= 1/frequency or

T = 1/f

→ Typical operating frequencies of switching regulator range from 10 to 50 kHz.

→ Lower operating frequency improves efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

 4. **Filter F1:**

→ It converts the pulse waveform from the output of the switch into a dc voltage.

→ Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.

→ The output voltage V_o of the switching regulator is a function of duty cycle & the input voltage V_{in}.

→ Vo is expressed as follows,

$$v_0 = \frac{t_{on}}{T} V_{in}$$

→ This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin.

→ This method of changing the output voltage by varying ton is referred to as a pulse width modulation.

→ Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform.

→ This method of varying the output voltage is referred to as frequency modulation (FM).

   ❖ Step – Down
   ❖ Step – Up
   ❖ Polarity inverting

5.7.1 MONOLITHIC SWITCHING REGULATOR [µA78S40]:

7. **Explain in detail on monolithic switching regulator with necessary pin diagrams.**

(or)

Explain the function of SMPS with neat waveforms and schema. (Apr/May 2019) (13 marks)

→ The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high-current, high voltage output switch, a power switching diode & an uncommitted op-amp.

→ Important features of the µA78S40 switching regulators are:

➢ Step up, down & inverting operation

➢ Operation from 2.5 to 40V input

➢ 80dB line & load regulations

➢ Output adjustable from 1.3 to 40V

➢ Peak current to 1.5A without external resistors

➢ Variable frequency, variable duty cycle device

→ The internal switching frequency is set by the timing capacitor CT, connected between pin12 & ground pin 11. The initial duty cycle is 6:1.

→ The switching frequency & duty cycle can be modified by the current limit circuitry, I_{PK} sense, pin14, 7 the comparator, pin 9 & 10.

Comparator:

→ The comparator modifies the OFF time of the output switch transistor Q1 & Q2.

→ In the step – up & step down modes, the non-inverting input (pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.

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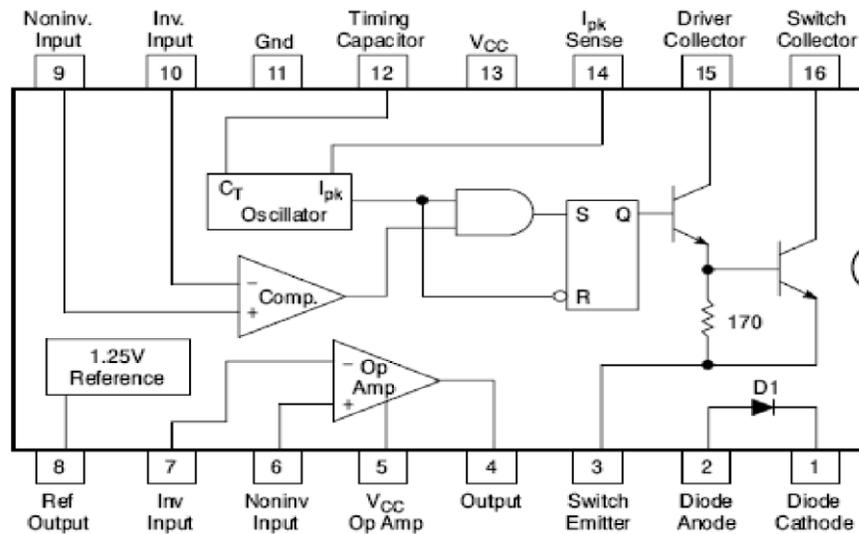
Fig 13: Functional block diagram of µA78S40
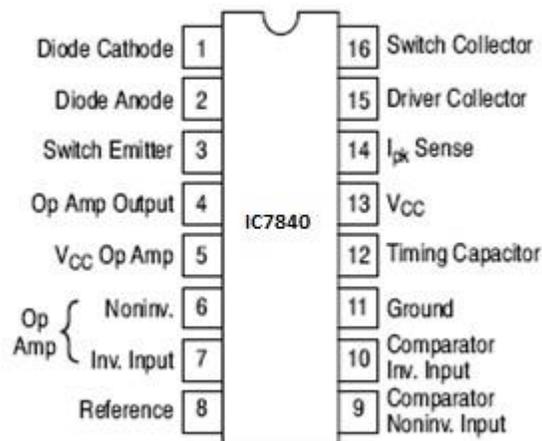
Fig 14: Pin Diagram

→ In the Inverting mode the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.

→ When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.

→ However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal, then the comparator output goes low.

→ In the LOW state the comparator inhibits the turn on of the output switching transistors.

→ This means that, as long as the comparator output is low, the system is in off time.

→ As the output current rises or the output voltage falls, the off time of the system decreases.

→ Consequently, as the output current nears its maximum Io (MAX), the off time approaches its minimum value.

→ In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between $I_{PK\ sense}$ & V_{cc}.

→ The current limit circuit is activated when a 330mV potential appears across Rsc.

→ Rsc is selected such that 330mV appears across it when the desired peak current IPK, flows through it.

→ When the peak current is reached, the current limit circuit is turned on.

→ The forward voltage drop, VD, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator.

→ Another important quantity used in the design of a switching regulator is the saturation voltage Vs

→ In the step down mode a —output saturation volt is 1.1V typical, 1.3VMAX.

→ In the step up mode a —Output saturation volt is 0.45V typical, 0.7 maximum.

$$R_{sc} = \frac{330mV}{Desired\ Peak\ Current}$$

→ The desired peak current value is reached; the current limiting circuit turns ON & immediately terminates the ON time & starts OFF time.

→ As we increase I_L (load current), V_{out} will decrease, to compensate for this, the ON time of the output is increased automatically.

→ If the I_L decreased then V_{out} increased, to compensate for this, the OFF time of the output is increased automatically.

5.7.2 Types of switching regulator

There are three types of switching regulator. They are:

➤ Buck or step-down regulator ($V_0 < V_i$)

➤ Boost or step-up regulator ($V_o > V_i$)

➤ Buck-Boost or inverter regulator or fly back regulator ($V_0 = -V_i$)

(i) Buck or Step – Down Switching Regulator:

→ This regulator, produces a dc output voltage lower than its input voltage.

→ C_T is the timing capacitor which decides the switching frequency.

→ Rsc is the current sensing resistance. Its value is given by

$$R_{sc} = \frac{330mV}{Desired\ Peak\ Current}$$

→ The Non-inverting terminal of the internal op-amp(pin9) is connected to the 1.3V reference (pin8).

→ Resistances R1 & R2 from a potential divider, across the output voltage Vo.

→ Their value should be such that the potential at the inverting input of the op-amp should be equal to 1.3V ref when Vo is at its desired level.

$$V_{(-)} = 1.3V = \frac{R_2}{R_1 + R_2} V_0$$
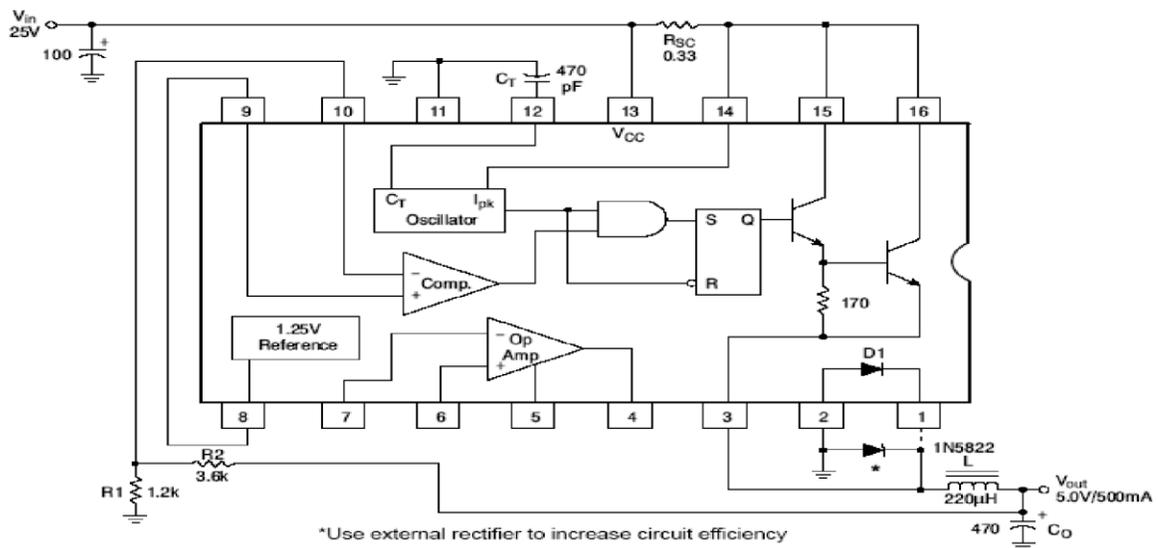
Figure 6. Step–Down Converter

Figure 15: Step down converter

(ii) Boost or Step – Up Switching Regulator:

→ Note that inductor is connected between the collectors of Q1 & Q2.

→ When Q1 is ON, the output is shorted & the collector current of Q1 flows through L.

→ The diode D1 is reverse biased & Co supplies the load current.

→ The inductor stores the energy. When the Q1 is turned OFF, there is a self induced emf that appears across the inductor with polarities.

→ The output voltage is given by,

$$V_o = V_{in} + V_L$$

$\rightarrow$ Hence it will be always higher than V_{in}& step up operation is achieved.

Figure 7. Step–Up Converter

With Q1 ON   with Q1 oFF
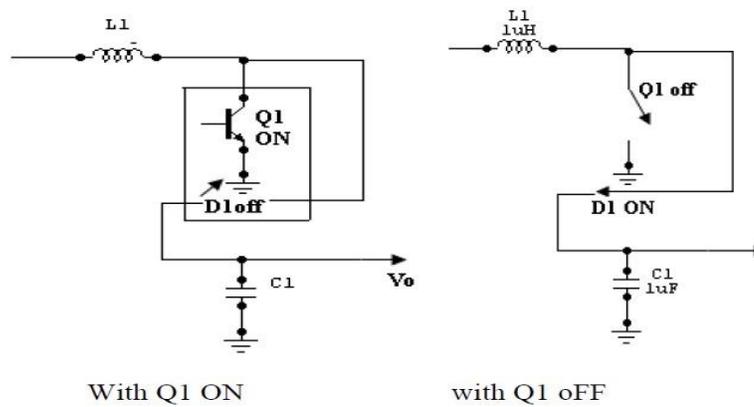
Figure 16: Step- up converter

(iii) Inverting Switching Regulator:

Inverting switching regulator converts a positive input voltage into a negative output voltage which is higher in magnitude.

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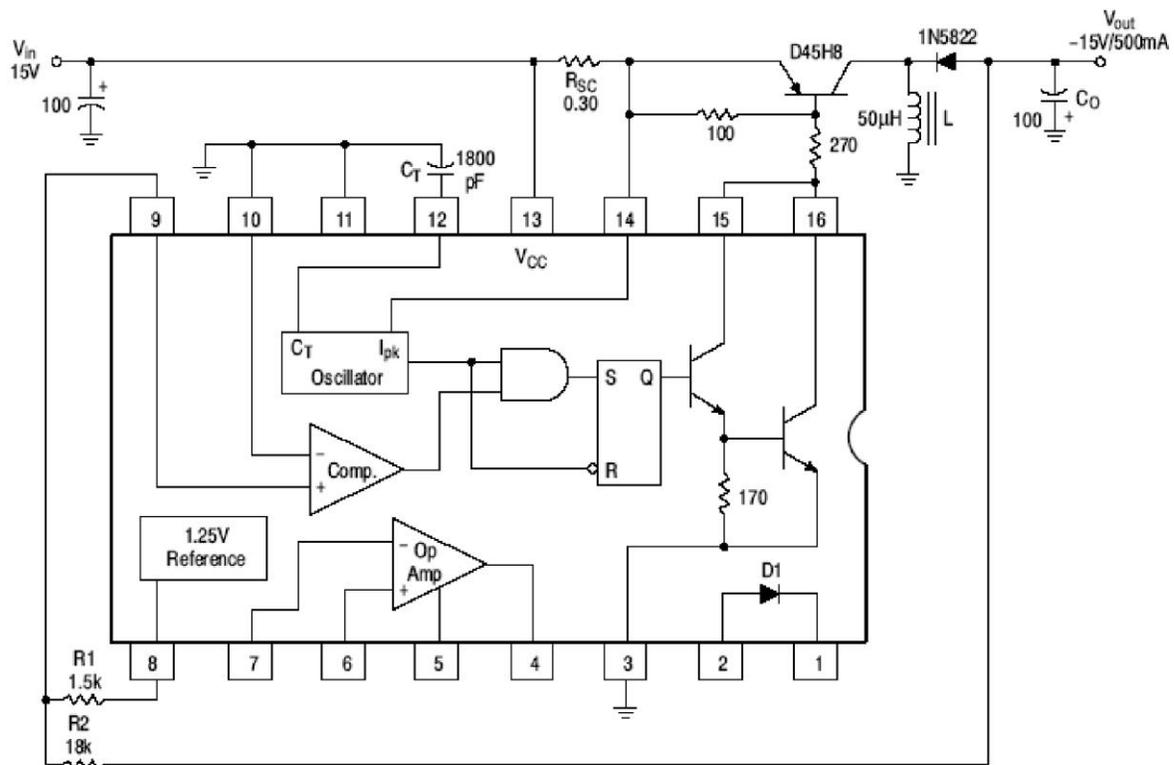
Figure 17: Inverting switching regulator
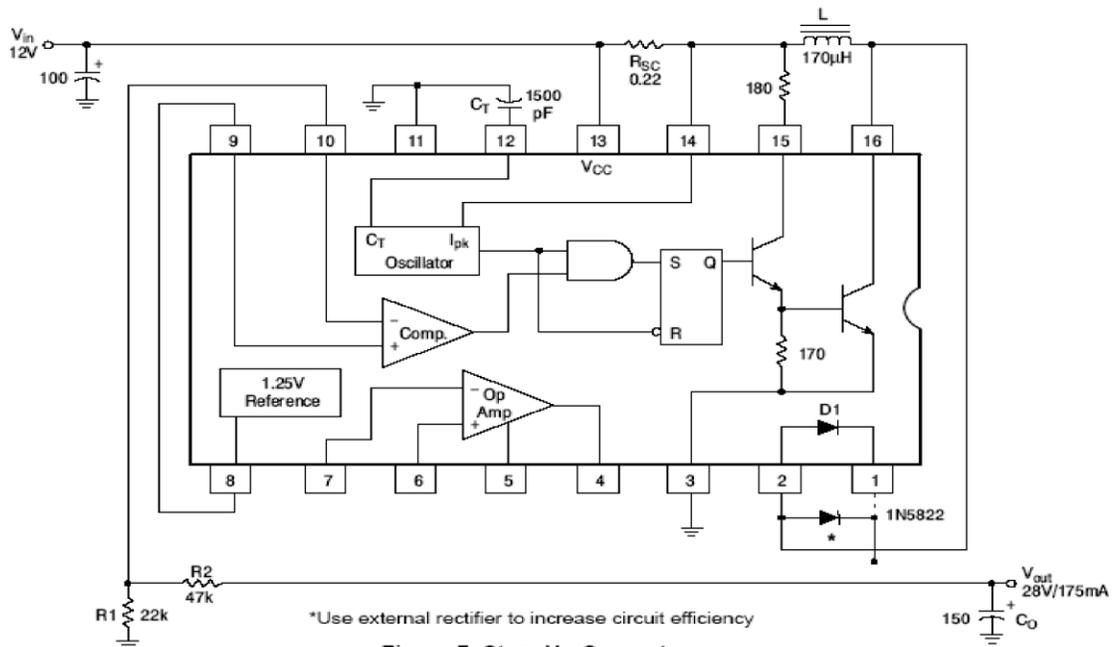
5.8 **FUNCTION GENERATOR IC 8038:**

8. **Discuss in detail on the function generator IC 8038. (13) [April/May 2017][Nov/Dec 2016][April/May 2015][April/May 2011]**

(or)

With neat figures explain the design of a circuit for performing (i) square wave generation (ii) sweep signal conversion (iii) clamped signal output [Apr/May 2019] (15 marks)

→ IC 8038 is an audio function generator.

→ This function generator IC is capable of producing sine, square and triangular functions.

→ IC – 8038 is an advanced monolithic IC designed using thin film resistors and schottky barrier diodes.

→ It consists of two current sources, two comparators, two buffers, a flip flop and a sine converter.

→ The pin diagram, block diagram and output waveforms are shown in figure below.

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5.8.1 Pin Diagram:

Fig 18: Pin diagram

5.8.2 Internal Block diagram:
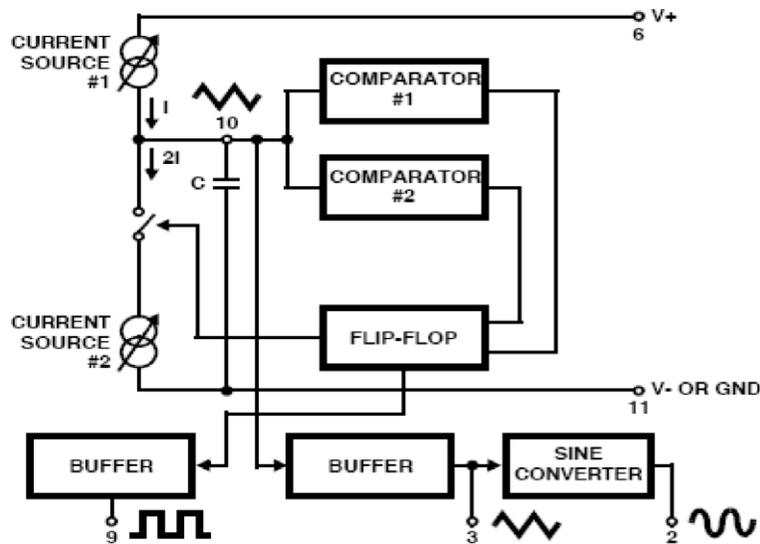
Fig 19: Functional block diagram of Function generator

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→ The triangular wave is generated by alternatively switching the capacitor between two current sources.

→ This triangle output is applied to comparators 1 and 2 and also to the sine wave converter through a buffer.

→ Two comparators with their reference voltage are compared with triangular wave and produces $\pm V_{sat}$.
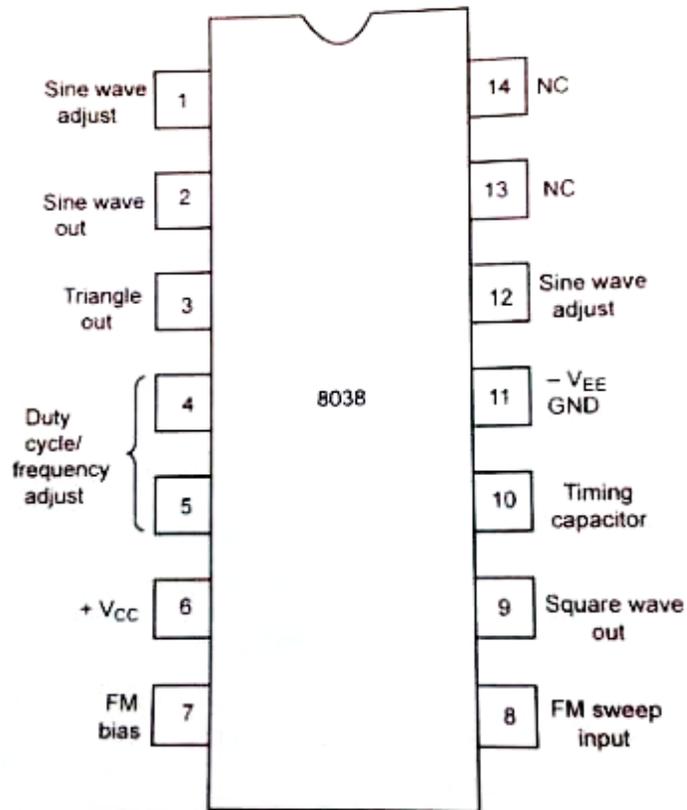
→ This saturation voltage is applied as logic input to a flip-flop which produces the square wave.

5.8.3 Output Waveform:
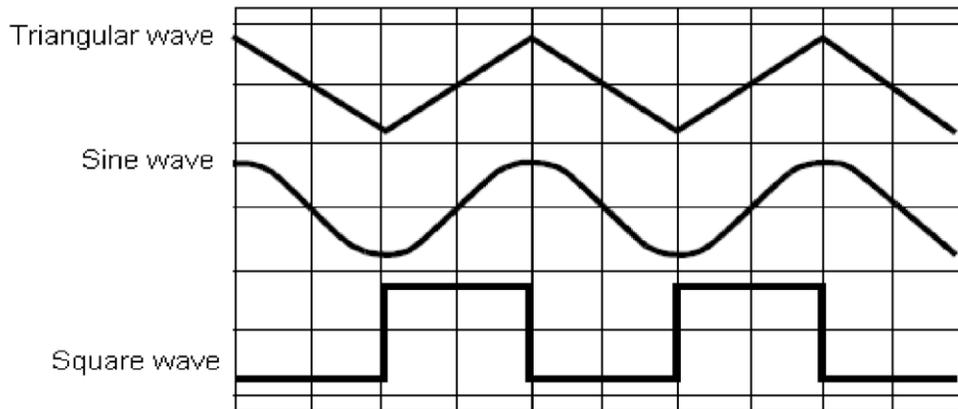
Fig 20: Output waveform

→ This square wave output is used to control the switching action of an electronic switch. The switch alternatively charges the capacitor and after a predefined time, it discharges the capacitor.

→ The 8038 pin diagram is a 14 pin DIP (Dual – inline – package). It is also available in plastic or ceramic package. The pin functions are given here.

5.8.4 Pin description:

Pin 1 & Pin 12: Sine wave adjusts:

→ Useful to achieve a sine wave distortion of less than 1%.

Pin 2 Sine Wave Output:

→ Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc.

Where $\pm 5V \leq Vcc \leq \pm 15$ V.

Pin 3 Triangular Wave output:

→ Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc.

Where $\pm 5V \le Vcc \le \pm 15$ V.

Pin 4 & Pin 5 Duty cycle / Frequency adjust:

→ The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors.

→ These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

Pin 6 + Vcc:

→ Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

Pin 7: FM Bias:

→ This pin along with pin no 8 is used to TEST the IC 8038.

Pin 9: Square Wave Output:

→ A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages.

→ This arrangement is very useful in making the square wave output.

Pin 10: Timing Capacitors:

→ The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

Pin 11: -VEE or Ground:

→ If a single polarity supply is to be used then this pin is connected to supply ground & if ($\pm$) supply voltages are to be used then (-) supply is connected to this pin.

Pin 13 & Pin 14: NC (No Connection)

5.8.4 Important features of IC 8038:

→ All the outputs are simultaneously available.

→ Frequency range: 0.001Hz to 500kHz

→ Low distortion in the output wave forms.

→ Low frequencies drift due to change in temperature.

→ Easy to use.

5.8.5 Parameters:

(i) **Frequency of the output wave form:**

→ The output frequency dependent on the values of resistors R1 & R2 along with the external capacitor C connected at pin 10.

→ If RA= RB = R & if RC is adjusted for 50% duty cycle then

$$f_0 = \frac{0.3}{RC}; \ R_A = R_1, R_B = R_3, R_c = R_2$$

(ii) **Duty cycle / Frequency Adjust: (Pin 4 & 5):**

→ Duty cycle as well as the frequency of the output wave form can be adjusted by controlling the values of external resistors at pin 4 & 5.

→ The values of resistors RA & RB connected between Vcc * pin 4 & 5 respectively along with the capacitor connected at pin 10 decide the frequency of the wave form.

→ The values of RA & RB should be in the range of 1kΩ to 1MΩ.

(iii)FM Bias:

→ The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.

→ The voltage V_{in} is the voltage between Vcc & pin8 and it decides the output frequency.

→ The output frequency is proportional to Vin as given by the following expression   For $R_A = R_B$ (50% duty cycle).

$$f_0 = \frac{1.5V_{in}}{CR_A V_{CC}} \qquad ; where \ c \ is \ the \ timing \ capacitor$$

→ With pin 7 & 8 connected to each other the output frequency is given by

$$f_0 = \frac{0.3}{RC}$$

Where R = RA = RB for 50% duty cycle.

This is because

$$V_{in} = \frac{R_1}{R_1 + R_2} V_{cc}$$

(iv)FM Sweep input (pin 8):

→   This input should be connected to pin 7, if we want a constant output frequency.

→   But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.

→   The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as,

$$f_0 = \frac{1.5V_{in}}{CR_A V_{cc}}$$

→ A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

UNIT – V (TWO MARKS)
APPLICATION ICs

1. **What is a voltage regulator?**

   A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

2. **Give the classification of voltage regulators.**

   The classification of voltage regulators are,
   - ➢ Series / Linear regulators
   - ➢ Switching regulators.

3. **What is a linear voltage regulator?**

   → Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region.

   → The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.

4. **What is a switching regulator?**

   → Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously.

   → This give improved efficiency over series regulators.

5. **What are the advantages of IC voltage regulators?**

   The advantages of IC voltage regulators are,
   - ➢ Low cost
   - ➢ High reliability
   - ➢ Reduction in size
   - ➢ Excellent performance

6. **Give some examples of monolithic IC voltage regulators. Or Give the seven output voltage option available in fixed voltage series regulator.[Apr/May 2019]**

   Some examples of monolithic IC voltage regulators are,
   - ➢ 78XX series fixed output, positive voltage regulators (5V,6V, 8V, 12V, 15V, 18V,24V)
   - ➢ 79XX series fixed output, negative voltage regulators (-5V,-6V, -8V, -12V, -15V, -18V,-24V)
   - ➢ 723 general purpose regulators.

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7. **What is the purpose of having input and output capacitors in three terminal IC regulators?**

   $\rightarrow$ A capacitor connected between the input terminal and ground cancels the inductive effects due to long distribution leads.

   $\rightarrow$ The output capacitor improves the transient response.

8. **Define line regulation. [Nov/Dec 2013][Nov/Dec 2014][Nov/Dec 2015]**

   $\rightarrow$ Line regulation is defined as the percentage change in the output voltage for a change in the input voltage.

   $\rightarrow$ It is expressed in milli volts or as a percentage of the output voltage.

9. **Define load regulation. Or Define load cell. [Nov/Dec 2014] [Nov/Dec 2015] [Apr/May 2019]**

   $\rightarrow$ Load regulation is defined as the change in output voltage for a change in load current.

   $\rightarrow$ It is expressed in mill volts or as a percentage of the output voltage.

10. **What are the different protection circuits used inside the monolithic IC regulator? [Nov/Dec 2014]**

    $\rightarrow$ Short-circuit protection

    $\rightarrow$ Thermal overload protection / thermal shut down

    $\rightarrow$ Current limiting and current sensing

    $\rightarrow$ Ripple rejection

11. **What is meant by current limiting?**

    Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

12. **Define duty cycle of a periodic pulse waveform.   [May/June 2013]**

    Duty cycle is the ratio of ON period (time) of pulse to total time period (ON and OFF period) of pulse. Duty cycle is often represented in percentage. It is given as

$$Duty\ cycle = \frac{T_{ON}}{T_{TOTAL}} = \frac{T_{ON}}{T_{ON} + T_{OFF}} X 100\%$$

13. **What are the limitations of IC723 general purpose regulator? [Nov/Dec 2012]**

    $\rightarrow$ Poor efficiency compared to SMPS

    $\rightarrow$ Spends more time on high dissipation transitions.

    $\rightarrow$ Larger transformer size and weight

    $\rightarrow$ Floating load must be used to get output greater than 37V.

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14. List the types of multivibrators.   [May/June 2014]

> ➢ Astable multi vibrator
> ➢ Mono stable multi vibrator
> ➢ Bi stable multi vibrator

15. Give the drawbacks of linear regulators.

The drawbacks of linear regulators are,

→ The input step down transformer is bulky and expensive because of low line frequency.

→ Because of low line frequency, large values of filter capacitors are required to decrease the ripple.

→ Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region.

16. What is the advantage of switching regulators?

→ Greater efficiency is achieved as the power transistor is made to operate as low impedance switch.

→ Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.

→ By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

17. What is an Opto-coupler IC?   [May/June 2014, 2018][May/June 2012][April/May 2011]

→ Opto-coupler IC is a combined package of a photo-emitting device and a photo-sensing device.

→ It has LED on the input side and photo diode on the output side.

→ It is used to couple input and output devices that are electrically isolated and optically coupled.

18. What are the types of Opto couplers?

The types of Opto couplers are,

> ➢ LED and a photo diode,
> ➢ LED and photo
>   transistor,
> ➢ LED and Darlington.

19. Give two examples of IC Opto-couplers?

Examples for Opto-coupler IC are,

$\rightarrow$ MCT 2F

$\rightarrow$ MCT 2E

20. Mention the advantages of Opto-couplers.

The advantages of Opto-couplers are,

$\rightarrow$ Better isolation between the two stages.

$\rightarrow$ Impedance problem between the stages is eliminated.

$\rightarrow$ Wide frequency response.

$\rightarrow$ Easily interfaced with digital circuit.

$\rightarrow$ Compact and light weight.

$\rightarrow$ Problems such as noise, transients, contact bounce, are eliminated.

21. List the characteristics of Opto-coupler.   [April/May 2008] [Nov 2017]

$\rightarrow$ Collector-emitter voltage

$\rightarrow$ Forward current and voltage

$\rightarrow$ Collector dark current

$\rightarrow$ Response time and bandwidth

$\rightarrow$ Current-transfer ratio (CTR)

22. What is an isolation amplifier?

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

23. What are the features of isolation amplifier?

The features of isolation amplifier are,

$\rightarrow$ Easy to use

$\rightarrow$ Ultra low leakage

$\rightarrow$ 18 pin DIP package

24. Define SMPS.   [Nov/Dec 2009] [May/June 2013][Nov/Dec 2016]

$\rightarrow$ SMPS is switched mode power supply.

$\rightarrow$ This power supply uses switching regulator with pass transistor acting as a control switch and is either operated at cutoff or saturation state.

$\rightarrow$ This type of regulator switch reduces power dissipation and acts as low impedance switch as compared to linear voltage regulators.
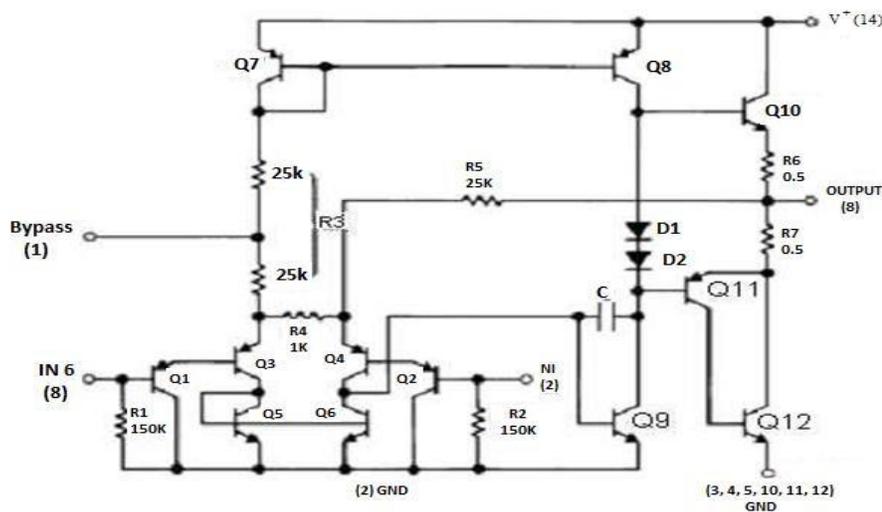
33

25. What is LM380?

→ LM380 is a power amplifier produced by national semiconductor.

→ It is capable of delivering 2.5 W min, to 8 ohm load.

26. What are the three different waveforms generated by IC 8038?   [Apr/May 2010]

The three waveforms are

→ Square wave

→ Triangle wave

→ Sine wave

27. Draw the internal circuit diagram of audio power amplifier.   [April/May 2010]

28. What are the features of MA78s40?

The features of MA78s40 are,

→ Step up, step down or inverting operation.

→ Operation from 2.5 to 40 V.

→ 80Db line and load regulation.

30.Comparison between variable voltage regulator and switching regulator. [May 2017]

Variable Voltage Regulator	Switching Regulator
Simple circuit configuration	More external parts required
Few external parts	Complicated design
Relatively poor efficiency	High efficiency
Considerable heat generation	Low heat generation

31. **How the frequency of triangular wave was can be obtained by IC 8038? [May 2017]**

The ICL8038 is a function generator chip, capable of generating triangular, square, sine, pulse and saw tooth waveforms. The circuit here is designed to produce waveforms from 20Hz to 20 kHz. The ICL 8038 has to be operated from a dual power supply.

32. What is the main function of voltage regulator?

The main function of voltage regulator is to provide a stable DC voltage for processing other electronic circuits.

33. What are the four main parts of voltage regulator?

- ➢ Reference voltage circuit
- ➢ Error amplifier
- ➢ Series pass transistor
- ➢ Feedback network

34. What is current limiting ability?

Current limiting ability refers to the ability of the regulator to prevent the load current from increasing above a preset value.

35. What are limitations of a linear mode or series regulator?

- → The input step down transformer is bulky and most expensive.
- → Since it operates at low line frequency, large values of filter are used.
- → Effectiveness is less.
- → More power is dissipated in the series pass transistors.

36. Define ripple rejection with respect t voltage regulators.

Ripple rejection is a measure of regulator's ability to reject ripple voltage and it is expressed in DB.

RR' = 20 log RR= 20 log Vr(out)/ Vr(in) DB.

37. What is a switching regulator?

Regulator which operates the transistor as a high frequency ON/OFF switch, so that the power transistor does not conduct current continuously is called switching regulator or switching mode regulator.

38. What are function generator?

Function generator is circuits used to provide basic waveforms with minimum number of external components. They are also called as waveform generators.

39. What are the basic configurations of switching regulators?

- ➢ Step- down or buck switching regulator
- ➢ Step- up or boost switching regulator
- ➢ Inverting type switching regulator

40. Why do switching regulator have better efficiency than series regulator?

Power transistor in a switching regulator does not conduct current continuously.

41. List the advantages of switching regulator.

➢ Very high value of resistors can be simulated.
➢ Low system cost.
➢ High accuracy
➢ Excellent temperature stability
➢ Complete active filters can be easily obtained.

42. List the important features of IC 723 regulator.

➢ Input voltage 40V max.
➢ Output voltage adjustable from 2 V to 37 V.
➢ Small size, lower cost.
➢ It has good line and load regulation.
➢ Input and output short circuit protection is provided.

43. Give the classification of regulators.

➢ Linear regulator
➢ Switching regulator

44. What are the limitations of linear voltage regulator?

➢ Low efficiency
➢ Large values of capacitors are required.
➢ It requires a bulky and expensive step- down transformer at the input.

45. Name the important performance parameters of 3 terminal IC regulators. Nov/Dec 2019

➢ Line regulation
➢ Load regulation
➢ Ripple Rejection Ratio (RRR)

46. Draw the PIN diagram of IC 723 regulator. Nov/Dec 2019

NC	1		14	NC
Current limit	2		13	Frequency compensation
Current sense	3		12	+Vcc
Inverting Input	4	IC 723	11	Vc
Non-Inverting Input	5		10	Vo
Vref	6		9	Vz
-Vcc	7		8	NC